Report No. 320

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ILLIAC III SCANNER ANALOG CIRCUITS

by

J. L. Divilbiss

April 10, 1969

DEPARTMENT OF COMPUTER SCIENCE
UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN · URBANA, ILLINOIS

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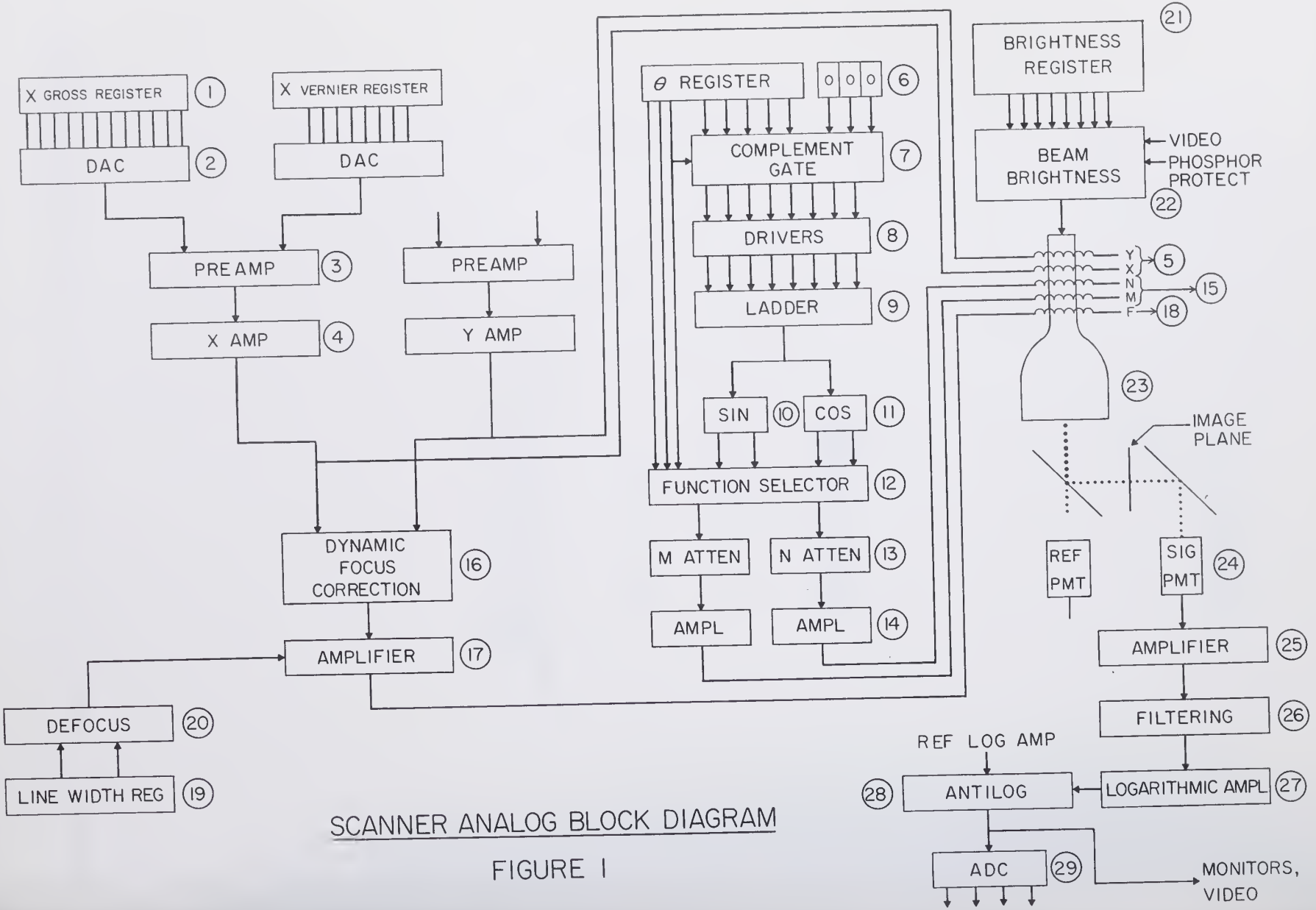


SCANNER ANALOG BLOCK DIAGRAM

FIGURE 1

1. INTRODUCTION

The scanners described in this report are mechanisms by which picture information can be converted to digital form for processing in the Illiac III computer. The simplest digital description of a picture results from breaking the picture into many tiny elements and then determining the opacity (assuming a photographic transparency) of each element. This is essentially the mechanism of televison scanning.

When pictures are processed by a digital computer it often happens that different areas within a picture not equally interesting. When this is true it is inefficient to scan the entire picture, both in terms of the time required to scan low-interest areas and in terms of storage required for picture elements. (A scan of 4096 x 4096 picture elements, each with 4 bits of gray scale information represents 67,108,864 bits, a figure much in excess of the storage capacity of available core memories.) In the Illiac III computer this problem is circumvented by making the scanning procedures dependent on picture information. As a simplified example of this, a picture might be scanned rapidly in a coarse mode and then scanned in a slower, fine-grain mode in areas of interest.

While a television scan (i.e., scanning every picture element in a systematic way) can be accomplished with a mechanical scanning device, a program controlled scan having flexibility as to step size, raster size, orientation, etc. cannot be accomplished mechanically. At present, the only satisfactory method of creating arbitrary scanning patterns is with the use of a cathode ray tube flying spot scanner, the device described here.

In this report the various analog circuits are divided into functional groups. The groups are further divided into "boxes", each of which represents an assembly of circuits for which input, output and

operating characteristics will be described. The general organization of the analog portion of an Illiac III scanner is shown in Figure 1. For clarity, a few boxes having only logic functions have been included. These are required for explanation of adjoining analog boxes.

The Deflection Group

The deflection group converts the digital coordinates specified by the scanner logic into magnetic deflecting fields which position the spot on the cathode ray tube face. Before describing in detail the various boxes in this group it will be necessary to make some general statements about limitations in digital-to-analog conversion (DAC) techniques.

Any DAC technique proposed for use with a CRT flying spot scanner must meet the following three general requirements. First, it must accept digital information in parallel and effect conversions fast enough to accommodate changes in the digital input. In the Illiac III system this means conversion must require much less than a microsecond. Second, the conversion must be linear, that is, equal increments in the digital input must produce equal increments in the analog output. Third, the conversion must be repeatable or, stated differently, must be stable in time. Our design goal in the Illiac III is a DAC output which is stable to one part in 40,000 over any thirty minute period. Note that there is no requirement for high absolute accuracy since spot position on the scanned image also depends on multiplicative factors such as CRT deflection sensitivity and optic ratios.

There are many interesting techniques for converting a digital signal into an analog voltage (or current) but if attention is restricted to high speed parallel converters only two basic schemes remain, voltage driven resistive ladders and weighted current summing networks. In both of these systems DC nonlinearities are not scattered at random but occur most prominently at major carry points. For example, in a four bit system the transition from 0000 to 0001 involves only the least significant bit and hence the error in the output can be no worse than the error contributed by this bit position. The transition from 0111 to 1000 involves all bit positions and can result in an output error which is the sum of the errors for each bit position. The difficulty of guaranteeing good linearity at the

major carry points generally limits converters of these two types to about twelve bits. Resolution of greater than twelve bits can be obtained over short intervals through the use of a composite system which uses the analog sum of two DAC systems as shown in Figure 2.

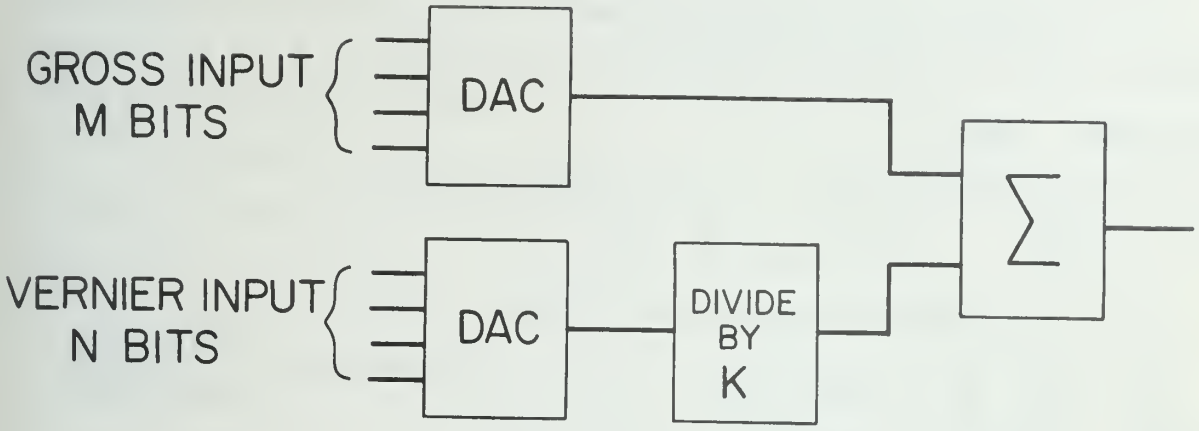


FIGURE 2

The division constant, K, can be selected so that the vernier bits are concatenated to the gross bits or so that they overlap the gross bits. Improvement in short interval resolution results from the fact that nonlinearities in the vernier DAC output are attenuated by the division constant, K.

Voltage driven resistive ladders of the type shown in Figure 3 are fairly simple to design and are capable of very high linearity and stability.

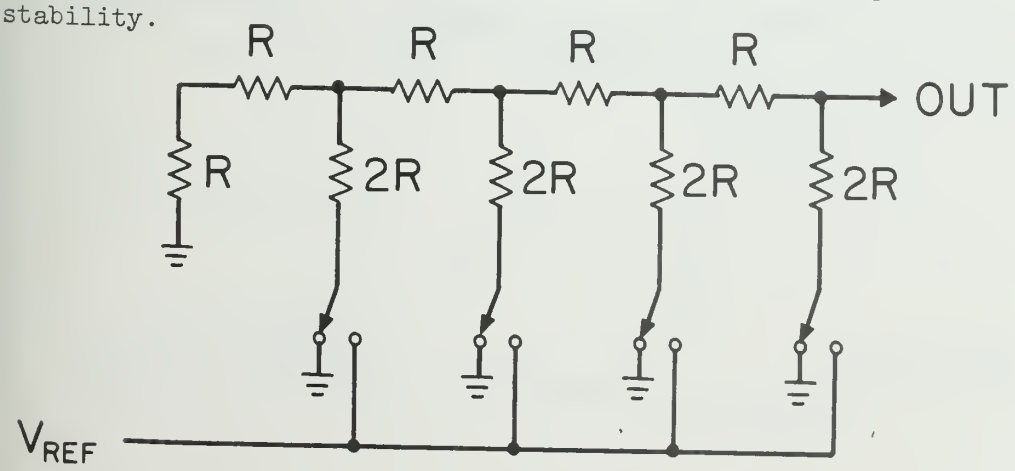


FIGURE 3

Unfortunately, circuits suitable for implementing the switch function are too slow for the Illiac III application. (Switches are usually realized with bipolar transistors, heavily saturated to make their effective resistance small compared to 2R. This heavy saturation greatly extends turn-off time.)

Weighted current summing systems of the type shown in Figure 4 represent another common approach to D to A conversion.

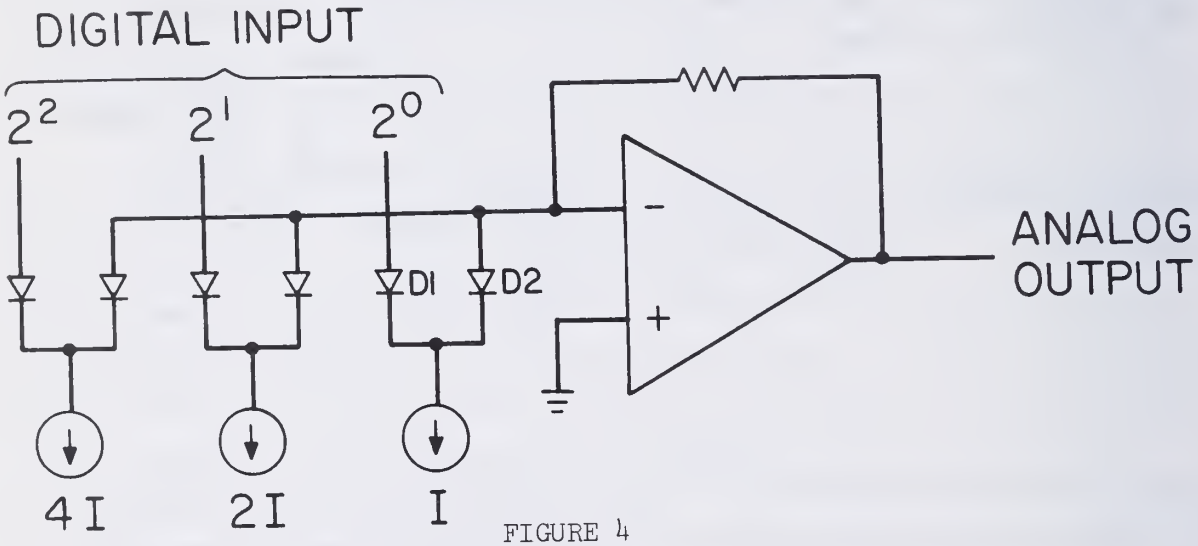


FIGURE 4

This system might equally well be called a current-diverter scheme. A negative voltage on the 2^0 logic input will reverse bias D1 and allow I to flow from the operational amplifier summing point; a positive voltage will reverse bias D2 and divert I to the logic signal driver. It is simpler and faster to divert the current than to turn the current generator on and off. In addition, greatest stability of a current generator results when the power dissipated in it is nearly independent of the digital input.

Box 2

Many practical problems accompany the design of a high speed DAC; these problems will be revealed by a point by point examination of the 1018-300-00 and 1018-306-00 cards which constitute box 2. Diodes D1 through D7 at the left side of Figure 5 make up an input protection network for the SN7475N integrated circuit buffer. This form of protection presupposes that the logic circuits driving these inputs are current limited for positive going signals. Thus, a conventional DTL card of the 1018-240-00 class is an appropriate driver, a 1018-214-02 is not.

The SN7475N quad flip-flop IC is part of an elaborate circuit designed to insure that the logic signals seen at the diverter diodes will change state simultaneously. This is an extremely important point which will bear further explanation. Assume an input state of 0111 for a four bit current diverter. If, in changing to a state of 1000, the one-to-zero transitions occur before the zero-to-one transitions (as is generally true with DTL positive logic) then the DAC will respond momentarily to a false input of 0000. The transient that this introduces into the system is, of course, directly proportional to the discrepancy in transition times. The example just given is shown schematically in Figure 6.

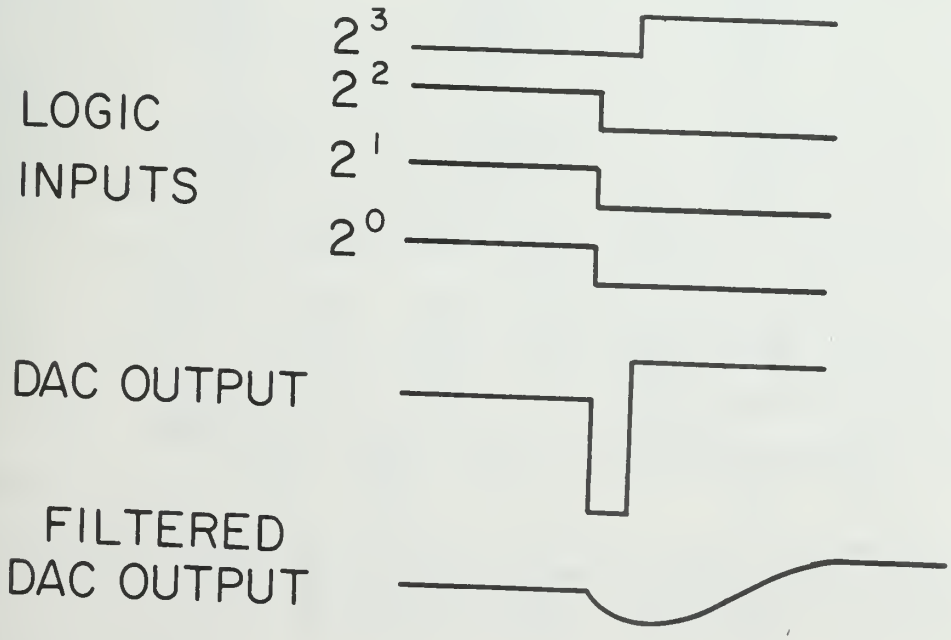


FIGURE 6

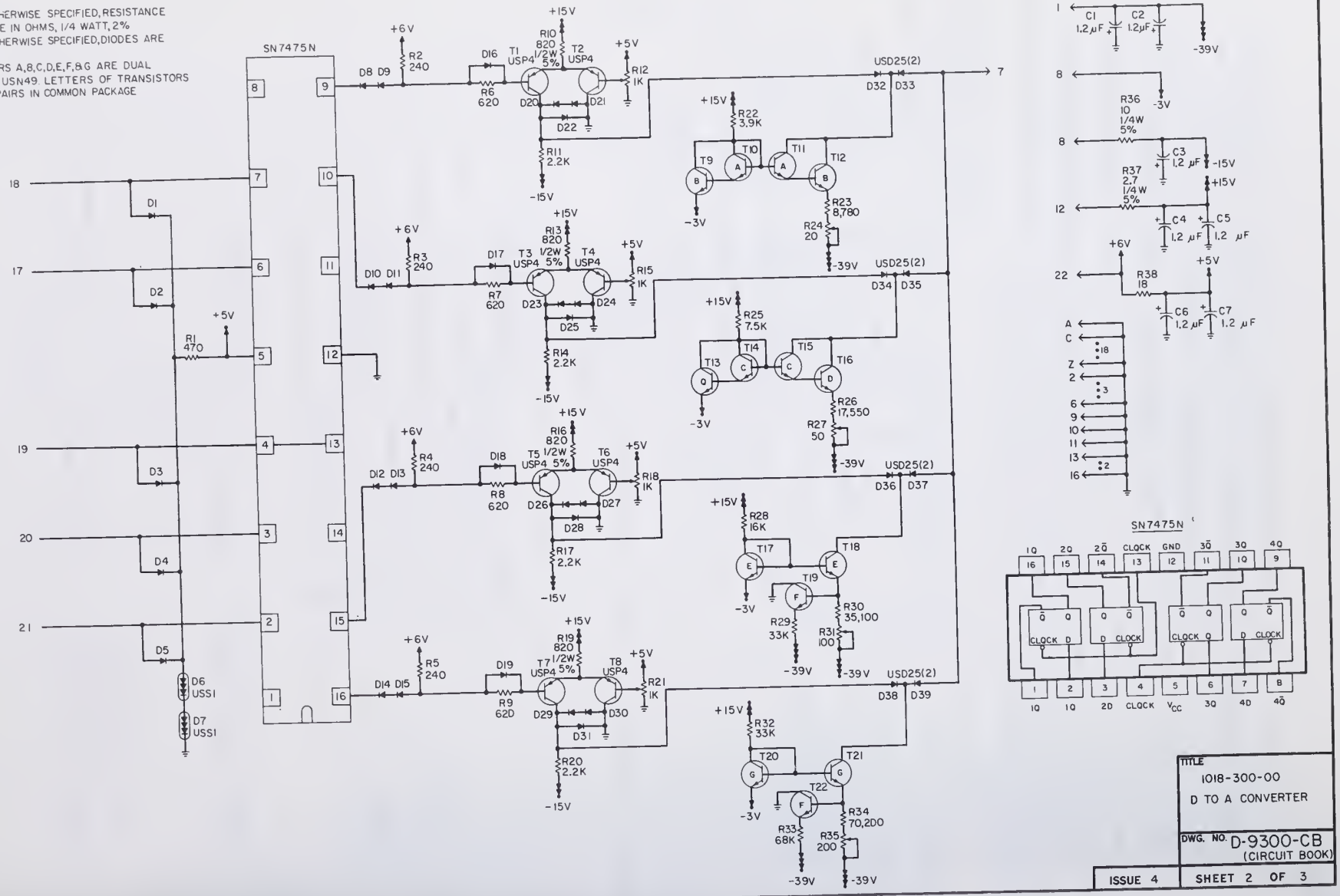

NOTES
1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, 1/4 WATT, 2%
2. UNLESS OTHERWISE SPECIFIED, DIODES ARE USD1.
3. TRANSISTORS A,B,C,D,E,F,&G ARE DUAL PACKAGED USN49. LETTERS OF TRANSISTORS INDICATE PAIRS IN COMMON PACKAGE
SN7475N
+6V
+15V
+5V
-15V
-3V
-39V
USD25(2)
R1 470
R2 240
R3 240
R4 240
R5 240
R6 620
R7 620
R8 620
R9 620D
R10 820 1/2W 5%
R11 2.2K
R12 1K
R13 820
R14 2.2K
R15 1K
R16 820 1/2W 5%
R17 2.2K
R18 1K
R19 820 1/2W 5%
R20 2.2K
R21 1K
R22 3.9K
R23 8,780
R24 20
R25 7.5K
R26 17,550
R27 50
R28 16K
R29 33K
R30 35,100
R31 100
R32 33K
R33 68K
R34 70,200
R35 200
R36 10 1/4W 5%
R37 2.7 1/4W 5%
R38 18
C1 1.2μF
C2 1.2μF
C3 1.2 μF
C4 1.2 μF
C5 1.2 μF
C6 1.2μF
C7 1.2 μF
T1 USP4
T2 USP4
T3 USP4
T4 USP4
T5 USP4
T6 USP4
T7 USP4
T8 USP4
T9
T10
T11
T12
T13
T14
T15
T16
T17
T18
T19
T20
T21
T22
D1
D2
D3
D4
D5
D6 USS1
D7 USS1
D8 D9
D10 D11
D12 D13
D14 D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D27
D28
D29
D30
D31
D32
D33
D34
D35
D36
D37
D38
D39
SN7475N
1Q 2Q 2Q̄ CLOCK GND 3Q̄ 3Q 4Q
1Q 1Q 2D CLOCK VCC 3Q 4D 4Q̄
TITLE
1018-300-00
D TO A CONVERTER
DWG. NO. D-9300-CB
(CIRCUIT BOOK)
ISSUE 4
SHEET 2 OF 3

FIGURE 5

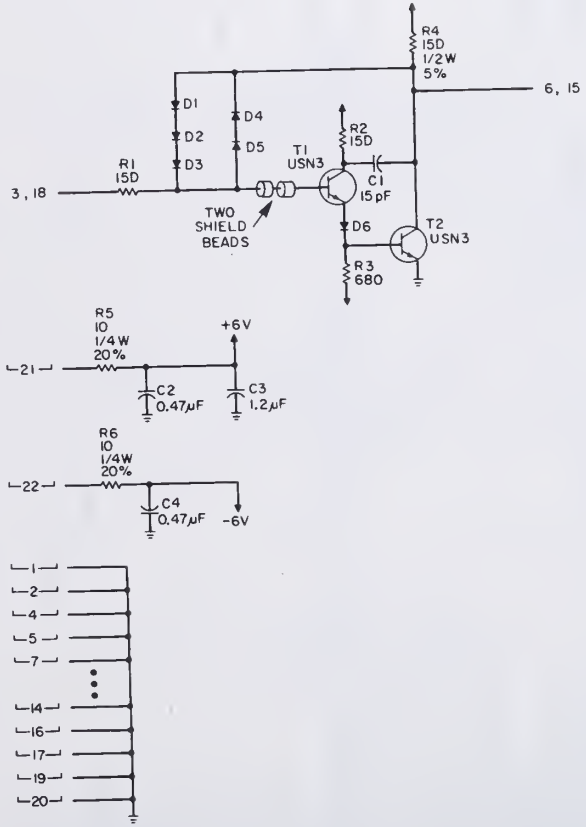
No simple means exist for removing the spike caused by asymmetry of transition times.* Any filter composed of linear elements can reduce the transient amplitude only at the expense of extending its duration. Nonlinear filtering might be possible but most nonlinear circuit elements have non-zero temperature coefficients and would therefore degrade the long term stability of the DAC. The answer, then, is to select components and to adjust circuits until transition simultaneity is achieved.

The first step in "cleaning up" incoming logic signals is to provide a data buffer physically near the diverter diodes. If the output of this buffer changes only on a clock signal then even very large transition discrepancies can be tolerated in the incoming data. In the particular buffer used here, the manufacturer guarantees the switching threshold for each flip-flop to be in the range of .8 volts to 2.0 volts. If flip-flops on a chip are not uniform, a slowly rising clock pulse will change the state of a low threshold flip-flop appreciably before changing the output of a high threshold flip-flop. This problem is minimized by providing a special nonsaturating clock driver circuit (the 1018-308-00 card) the output of which traverses the .8 volt to 2. volt region in one nanosecond.

The high speed clock (shown in Figure 7) is a fairly conventional Darlington configuration with diode feedback to prevent both saturation and cutoff. For a logic one input (nominally +6 volts) the output falls to +.7 volts at which point diodes D4 and D5 conduct to prevent saturation. Similarly, for a logic zero input, D1, D2 and D3 limit the output voltage to +4 volts. Prevention of cutoff contributes only very slightly to circuit speed but does limit the output to a value compatible with IC TTL logic. R4 is as small as is consistent with the dissipation rating of T2 in order to speed the output risetime. The shielding beads, R2 and C1 are required to prevent ringing. At first glance it may appear that the +.7 volt output of the clock is perilously close to the +.8 volt threshold limit of the IC buffer. This is not a problem if the clock and DAC cards are located in adjacent card positions.

*The high speed DAC system used in the Bell Telephone Laboratories pulse code modulation system employs "resampling", a moderately complex method suppressing transients at all transitions. The method is successful in their application but requires a constant encoding rate and is, therefore, not applicable here.

NOTES
1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, 1/4 WATT, 2%
2 UNLESS OTHERWISE SPECIFIED, DIODES ARE USDI.



TITLE	1018-308-00 HIGH SPEED CLOCK DRIVER
DWG NO.	D-9380-CB (CIRCUIT BOOK)
ISSUE 1	SHEET 2 OF 3

FIGURE 7

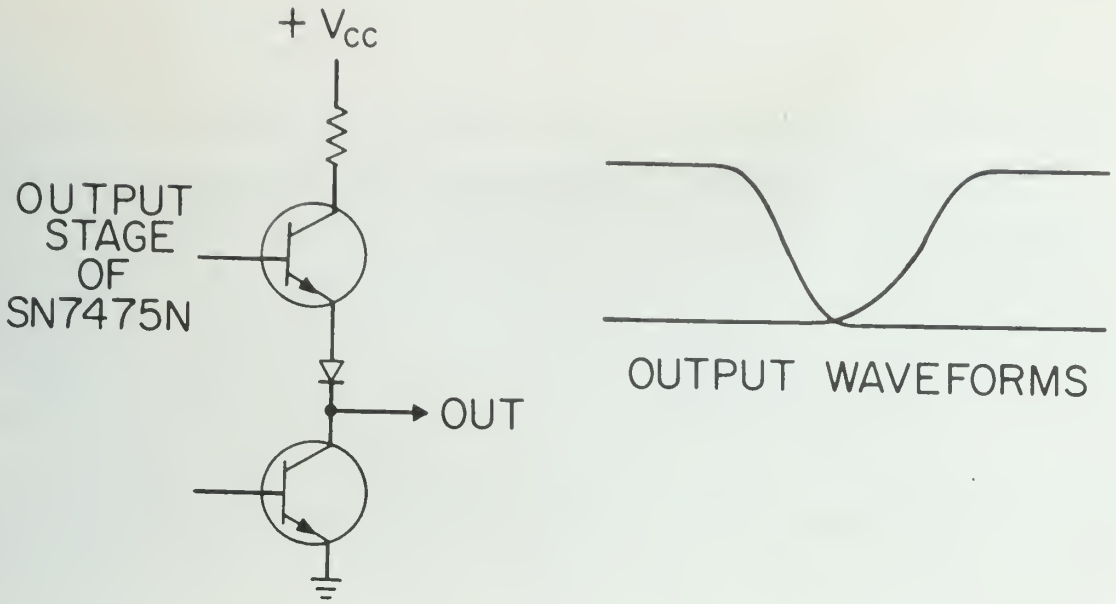


FIGURE 8

As is indicated in Figure 8, output from the SN7475N has a transition asymmetry of about 14 nsec. measured at +2 volts. We have employed a three pronged approach in reducing this value. First, R2 (Figure 5) provides fairly heavy loading in a direction which speeds the positive transitions. Second, D16 and R6 are oriented to slow the negative transitions at the base of T1 while having minimal effect on the positive transitions. Third, R12 adjusts the threshold of the differential amplifier to compensate for component variations. The entire adjustment procedure for the 1018-300-00 card is contained in Appendix I.

An inherent problem with current diverter systems is that the switching signal is capacitively coupled to the analog summing point through the diverter diodes. This problem is shown in simplified form in Figure 9.

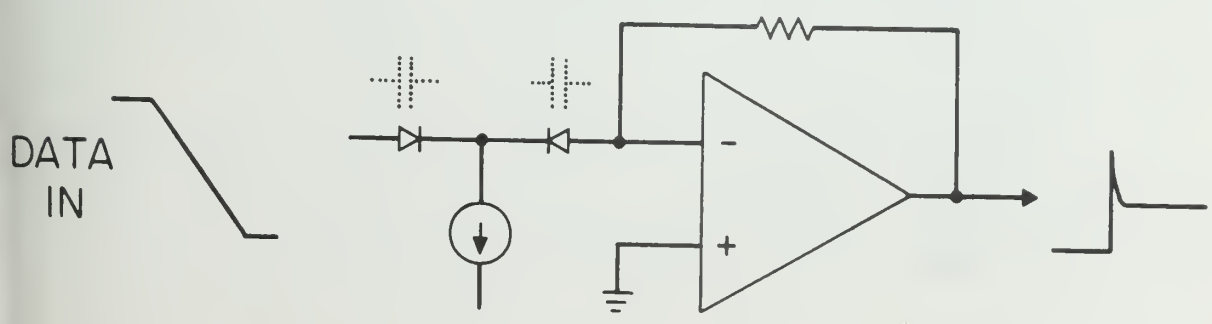


FIGURE 9

Here again a variety of techniques is needed to minimize this source of error. R10 and R11 are chosen to provide T1 collector rise and fall times of about ten to fifteen nanoseconds each. Symmetry of rise and fall times at this point allows partial cancellation of capacitive feedthrough for some data changes, such as 0001 to 0010. The principal reason for controlling rise and fall times, however, is to limit the capacitivly coupled error current, $C \frac{dv}{dt}$, by limiting $\frac{dv}{dt}$. Limitation of rise and fall times here is most easily accomplished by selecting moderately slow transistors for T1 and T2.

Since the output of the 1018-300-00 card is connected to the input of an operational amplifier the switching signal supplied to the diverter need swing only slightly above and below ground. Diodes D20 and D21 limit the negative swing of the driver stage and help to limit the duration of the $C \frac{dv}{dt}$ coupled error current. Diode D22 limits the positive swing for the same reason and in addition prevents T1 from saturating. It will be made clear in a following section why the positive and negative clamps have unequal numbers of diodes.

In previous paragraphs the error current was given as "$C \frac{dv}{dt}$" without explicit reference to which capacitance was involved. In point of fact, for a typical diverter system the greatest source of signal-induced error results not from diode capacitance but rather from charge stored in the diverter diodes. Happily, it is now possible to buy hot carrier diodes having almost zero charge storage when compared to conventional high speed silicon logic diodes. (The Hewlett-Packard 5082-2800 has less than one picocoulomb of stored charge at the current levels used in the 1018-300-00.) It is no exaggeration to say that high speed current diverter systems are feasible <u>only</u> if hot carrier diodes are used for the diverters.

Although hot carrier diodes eliminate the stored charge problem they do have junction capacitances on the order of one picofarad. This means that the previously developed arguments for shaping the driver waveform are still valid. The exact extent of capacitivly induced currents is

difficult to determine since diode capacitance varies with bias. Also, there are wiring capacitances and the finite impedance of the current source to confuse the issue. (A reverse biased diode and a length of wire may constitute a capacitive divider network, with the division ratio constantly changing as the diode bias changes.) Finally, the input to the operational amplifier is a virtual ground only as an average. For transient conditions it may depart substantially from ground.

The current generator for the most significant bit can best be explained by starting with a very simple current generator and then adding features.

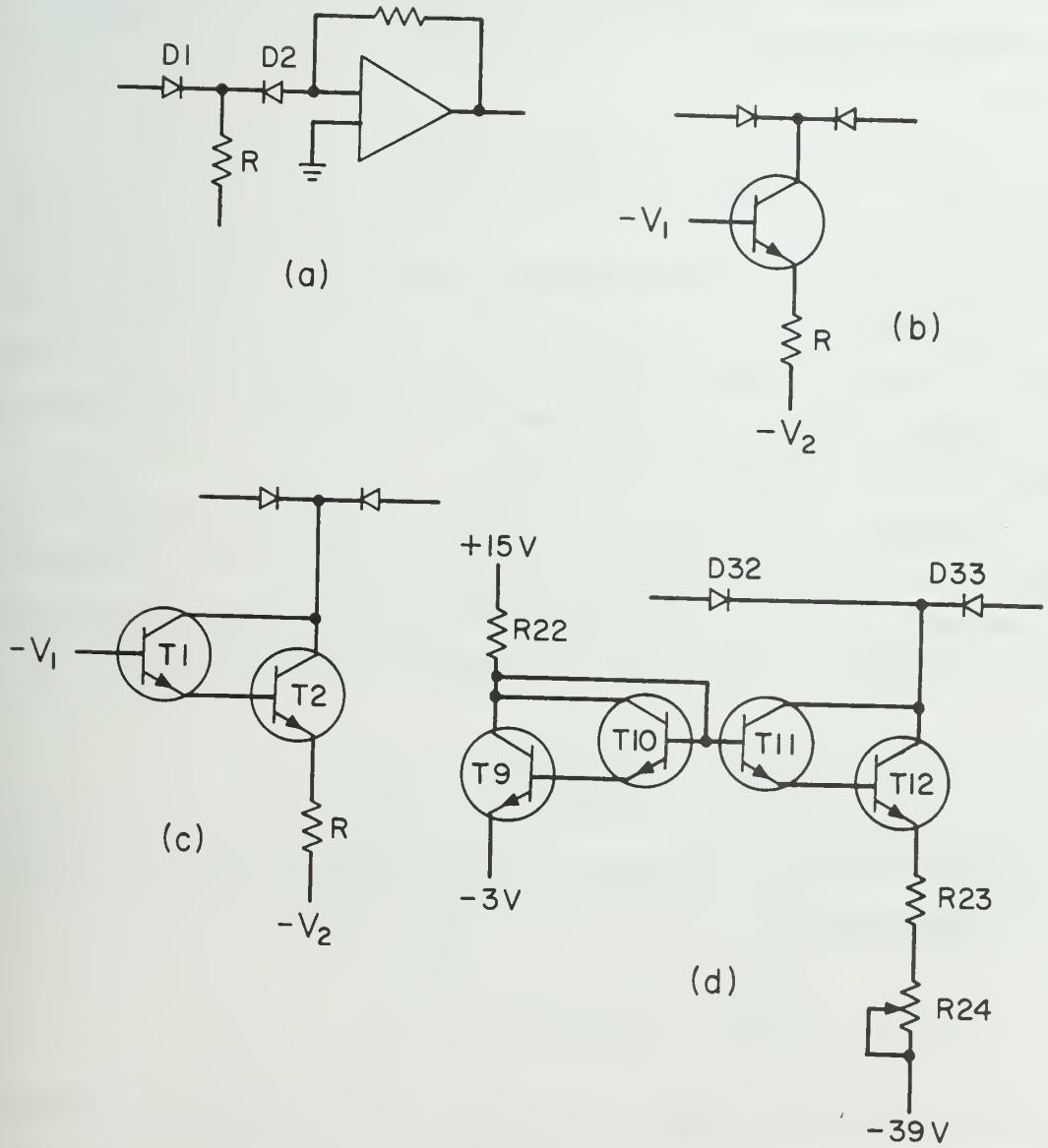


FIGURE 10

The current generator of 10a fails only because the voltage drop across D2 depends on temperature. This effect can be partly offset by making —V very large but it is not feasible to achieve one part in 40,000 stability this way. The circuit of 10b adds another problem without solving the previous one; the collector current depends on the base current which is temperature dependent. Base current for the Darlington complex of 10c is a negligible factor but voltage across R depends on the combined base-emitter drops of T1 and T2. In the final configuration, 10d, two transistors have been added to compensate for thermal variations in V_{BE}. T10 and T11 are contained in one dual package, T9 and T12 in another. The manufacturer's specification sheet for this dual transistor (Sprague TD101) lists a typical base-emitter voltage tracking of

$$|\Delta(V_{BE1} - V_{BE2})_{TA}| = 6\mu V/°C$$

which would appear to give nearly perfect compensation. In practice, things are not quite this rosy since the specification above is stated in terms of changes in the ambient temperature. Unless care is exercised, much larger $|V_{BE1} - V_{BE2}|$ tracking errors will result from unequal junction heating caused by unequal collector dissipations.

Tests were made on a small sample of TD101's to establish two important thermal parameters not given in the manufacturer's data sheet. The first of these measured the change in V_{BE1} which results from changing the power dissipation while keeping the emitter current constant.

$$\frac{\Delta V_{BE1}}{\Delta P_{C1}} = .36 \text{ mv/mw}$$

The second test measured the change in V_{BE2} for a unit change of dissipation in the #1 transistor.

$$\frac{\Delta V_{BE2}}{\Delta P_{C1}} = .12 \text{ mv/mw}$$

The ratio of these two thermal coefficients can be regarded as a measure of the thermal coupling between the two transistors. A number of caveats

are appropriate here. Thermal properties were measured only over the very restricted range of power dissipations appropriate to this application and should not be regarded as applying generally. In addition, the thermal coefficients given are average values; even within a sample of 5 dual units variations of $\pm$ 20% were seen.

Finally, thermal time constants for this device are quite long. For an abrupt change in collector dissipation of 15 mw, approximately one minute is required before the base-emitter voltage settles to within one mv of its final value. (A change of 15 mw is not typical in this application but was used in order to make the V_{BE} shift large enough to measure conveniently.)

Armed with these thermal coefficients, we can now calculate the V_{BE} shift of T12 which results from changing input data. Examination of Figure 5 shows that the collector of T12 cannot go more negative than the drop access D33 nor more positive than approximately zero, a total swing of about .6 volts. For an emitter current of 4.096 ma this means a variation in collector dissipation of 2.5 mw and a V_{BE} shift of .9 mv. It is true that this V_{BE} shift will be partly compensated by a shift in the V_{BE} of T9 but on a practical time scale the compensation is not helpful. For the power supplies specified, a .9 mv V_{BE} shift affects the current by one part in 40,000. Neither T10 nor T11 has enough internal dissipation to have any influence on their base-emitter drops; they must be paired, however, to cancel variations due to changes in the ambient. T9 dissipates a steady 5 mw independent of the data input.

The only remaining requirements for a stable current generator are a high stability power supply and a stable emitter resistor. Note that the critical current-determining voltage is from -3 to -39, not -39 to ground. For this reason two power supplies are connected in series here, an ordinary

laboratory supply for -3 volts and an ultra stable -36 volt supply in series to provide the -39 volt return. R23 is a Vishay film resistor with a temperature coefficient of 1 ppm. R 24 has purposely been made very small to simplify "fine tuning" of the current and to minimize the thermal drift added by this component. The cermet pot used here has a tempco of about 100 ppm.

The next most significant current source is essentially identical to the one just described. Note that R25 has been selected to make the emitter current of T13 equal that of T16.

For the two remaining current sources on the 1018-300-00 card a slightly different technique of thermal compensation is used. Instead of using a Darlington connection to make the base current negligibly small, a dummy transistor is used to compensate for variations in base current. If T18 and T19 are selected for the same DC beta, then the collector current of T18 will equal the current through R30. (R29 was chosen to make the emitter currents of T18 and T19 equal.) T18 has a base current of less than 5μA and exhibits a variation of about .03μA per degree Celcius. If the base currents of T18 and T19 track to within 10% for reasonable changes in the ambient then a ten degree change in ambient will introduce an error of about one part in 260,000 of the full scale output of the DAC. No allowance need be made for data-dependent collector dissipation since the dissipation of T18 differs by only .6 mw for the two logic states.

The complication of a second current generator design was not introduced for the trivial saving in transistors that it makes possible. Rather, the second design is used because the Darlington connection is not satisfactory for small currents. As is well known, the Darlington gains its high equivalent beta at the expense of sluggish operation. For our purposes it is very much as if a small capacitor were connected from the collector of T12 to ground. Positive excursions of the driver will quickly charge this capacitance through D32 but negative excursions merely allow the charge to be drawn off by the constant 4.096 ma current source. Obviously, for less significant bits with smaller currents the associated

time constant is longer. The second current generator design reduces this time constant problem but does require a more complicated transistor selection procedure. This procedure is given in Appendix II.

If speed were no object the remaining eight current generators (packaged on two additional printed circuit cards) could be designed using the techniques of the preceding paragraphs. Speed is an object, however, and some way must be found to avoid the long time constants associated with stray capacitances and very small currents. (Current for the least significant bit would be only 2μA.) Figure 11 illustrates the essential mechanism for avoiding very small currents at the diverter diodes. A very useful by-product of this approach is that the three DAC cards are identical, thus simplifying production, testing and stockpiling of spares.

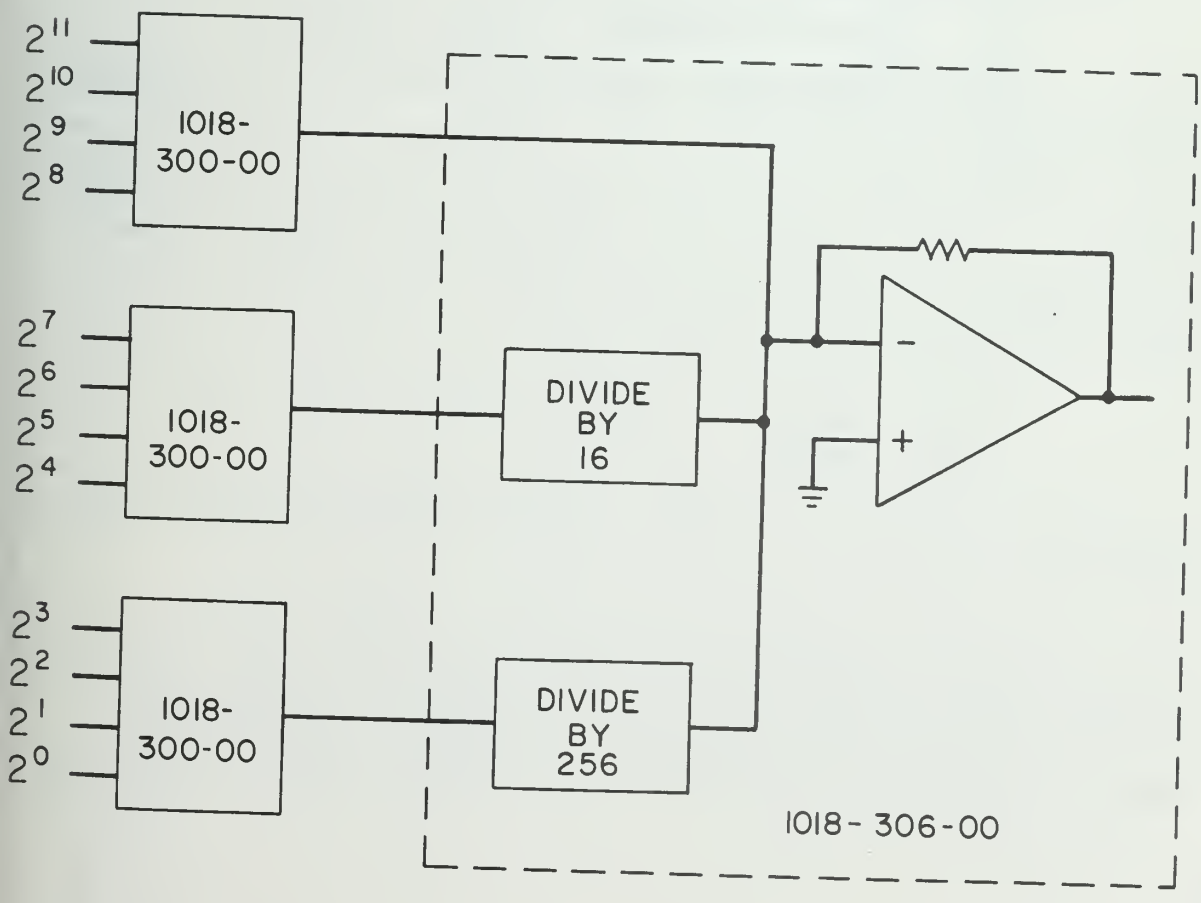
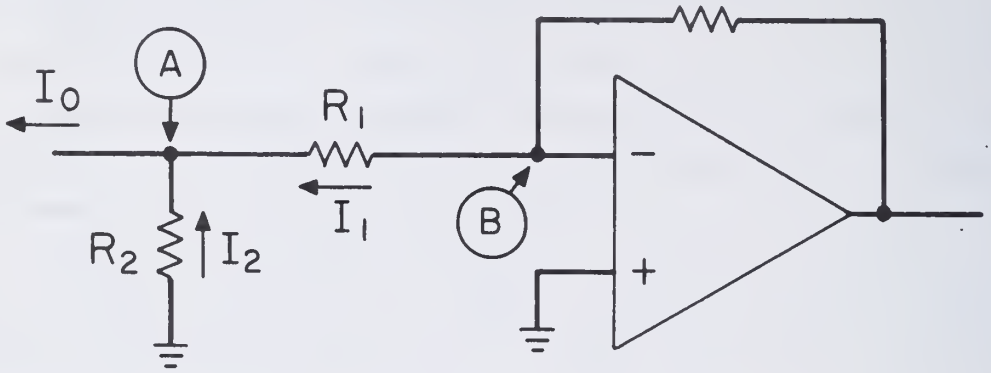


FIGURE 11

The current division shown in Figure 11 is accomplished by simple resistor networks which none the less merit some discussion. In Figure 12 we see the divider network reduced to its barest essentials.



I_0 IS FROM 1018-300-00 CARD, 0 TO 7.68 MA

FIGURE 12

For $I_1 = I_o/N$ it follows from Ohm's law and the assumption of a "perfect" operational amplifier that $R_1 = R_2(N-1)$. Actually, the input of the Analog Devices 149A can vary by 150μV with changes in the data and room temperature variations. R1 must be chosen large enough so that a nonzero voltage at B does not result in an appreciable error in I_1. If R1 is made 1300 ohms the maximum error due to amplifier offset is

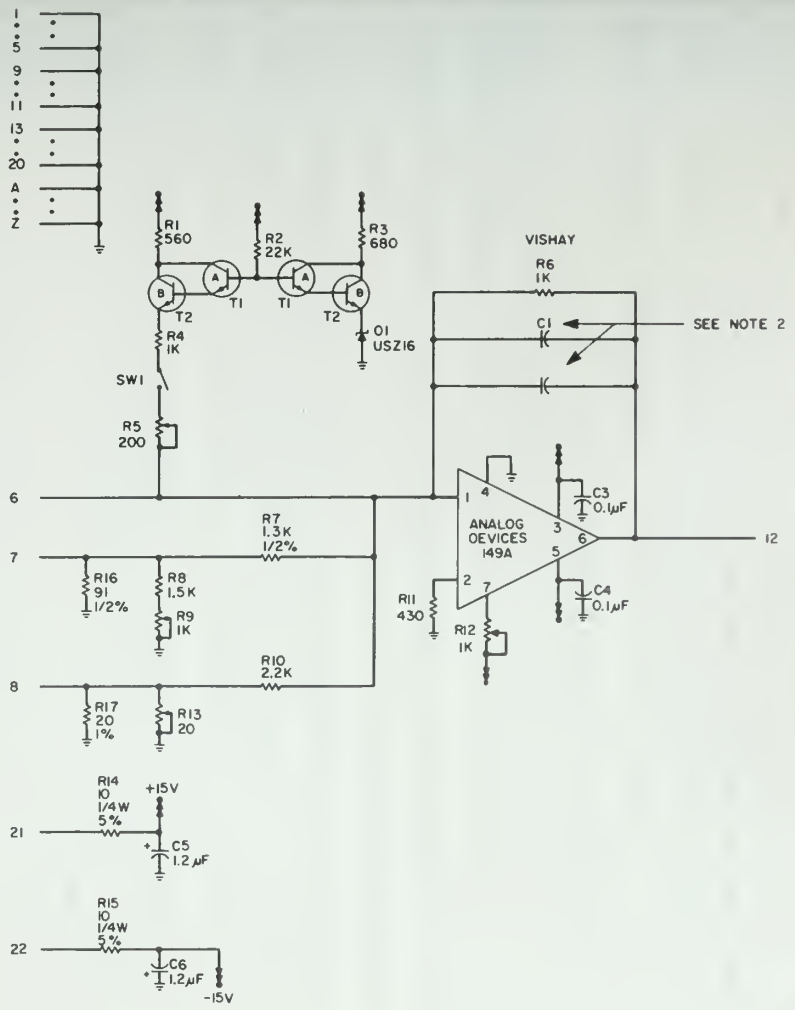
$$\left(\frac{N-1}{N}\right) \quad \left(\frac{150\mu V}{1300\Omega}\right) \quad = .108\mu A$$

or about one twentieth of the LSB. A division ratio of 16 yields an R2 of 86.67 ohms.

Of course, the addition of resistive dividers means that the two less significant DAC cards do not work into zero impedance loads (as does the most significant card) and this warrants a reexamination of Figure 5. The output of each DAC card is a current ranging from zero to

NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, 1/4W, 2%
2. CAPACITOR VALUES FOR C1 & C2 TO BE SPECIFIED.
3. ALL TRANSISTORS ARE USN 49 OR USN50.
4. TRANSISTORS A & B INDICATE COMMON HOUSING.



	1018-306-00
	OP AMP FOR DAC
	D-9360-CB (CIRCUIT BOOK)
ISSUE 2	SHEET 2 OF 3

FIGURE 13

7.68 ma. The middle DAC card sees the 81.25 ohm impedance of the divide-by-sixteen network and thus develops an output swing of zero to -.624 volts. Now it becomes clear that the use of two diodes for the negative clamp (D20 and D21) is necessary to insure proper switching of current in the middle DAC position. The second of the two diodes could have been omitted for cards used in the most significant position but it is simpler logistically to make all cards alike.

The selection of resistors for the divide network is bounded by the following two restrictions: 1), R1 must be large enough to reduce offset errors to an acceptable level and 2), R1 must be small enough to limit the voltage swing at the DAC card.

Precision of the division ratio can be obtained either by the use of high precision resistors or by using less precise but adjustable networks.* As is clear from Figure 13, we have elected the latter approach. The divide by sixteen network allows an adjustment of approximately $\pm$ 1.5% around the center value. Since R9 is a twenty turn pot the adjustment is quite simple to make.

The divide by 256 network is simple to design since the large ratio results in a small input impedance. Voltage swing for the DAC card connected to this input is only about 66 mv.

With switch 1 open, output of the operational amplifier ranges from zero to +8.190 volts, the current to voltage conversion ratio being determined by R6, a .01%, 1K resistor. (This range was selected so that all output voltages would be integer multiples of 2 mv, a choice that materially simplifies adjustment.) For reasons which will become clear

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*Corning Glass tin oxide resistors having 1% accuracy, good long term stability and a tempco of 50 ppm cost about seventeen cents. Vishay thin film resistors of .01% accuracy and 1 ppm tempco are about eight dollars each.

shortly, the pre-amplifier (box 3) requires an input range of zero to some negative voltage. This polarity discrepancy could be resolved with a unit-gain inverter but a simpler solution is to translate the op amp output by 8.190 volts. With switch 1 closed, R5 can be adjusted to provide +8.190 mA into the input terminal of the op amp, thus shifting the output range to zero to -8.190 volts.

The current generator used to effect this output translation is similar to the current generators on the 1018-300-00 card. If base emitter voltages track, the emitter voltage of T1 will equal the drop across D1, a 9V zener with a .01%/^{o}C temperature coefficient. Note that R3 establishes an operating current of about 8 ma for D1 and that R1 must be slightly smaller than R3 to avoid saturating T1. Emitter currents and collector dissipations are closely matched and do not vary with input data. Adjustment procedure for the 1018-306-00 card is given in Appendix 1.

A subtle source of error in precision DAC's results from unintended coupling of logic and analog circuits through common ground circuits. This situation is illustrated in greatly simplified form in Figure 14.

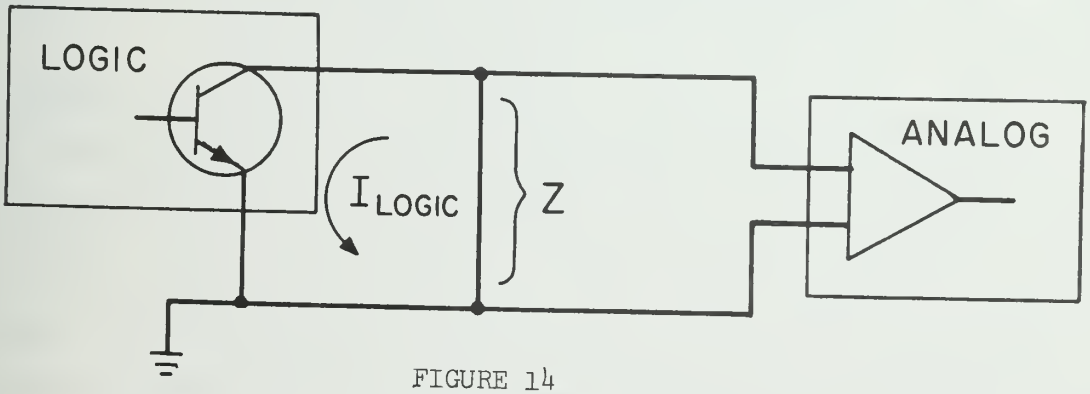


FIGURE 14

The analog circuit in this case responds to a "logic noise" voltage equal to the product of the logic current variation and the impedance of that part of the ground system common to both loops. The common Z can be minimized by placing clock, DAC and op amp cards in adjacent card slots and by wiring at least twelve parallel ground paths between cards. This

plurality of ground wires creates, in effect, a local ground plane on the wiring side of the connectors.

BOX 3

The deflection pre-amplifier shown in Figure 15 is based, at least historically, upon a Digital Equipment Corporation design. The knowledgeable reader will quickly discover that the circuits used here are less precise and stable than the DAC circuits. A partial justification for this will be given following the description of the deflection amplifier.

The 1018-280-00 card can be regarded as an operational amplifier with input at the base of T5, push-pull outputs from the emitters of T1 and T2. Before examining the feedback connections we might look at the circuit elements which affect open loop gain. T5 and T6 are the two halves of a 2N2060 dual transistor connected as a differential amplifier, common emitter current being supplied by T7. A positive signal voltage at the base of T5 increases the emitter current of T5 and decreases that of T6 by the same amount. If we momentarily ignore R4, we see that the collector load of T5 is the input impedance of an emitter follower or approximately R3 multiplied by the beta of T2. Thus, the voltage swing on the collector of T5 is approximately $\Delta I \times 75K$ (for $\beta = 50$), this swing being carried to the output pins via two emitter followers.

The voltage across R4 is essentially a constant, the combined drop of a zener diode and a base-emitter junction. Since the current in R4 does not depend on the collector voltage of T5, this resistor does not parallel the already computed effective collector load of 75K. Instead, R4 serves as a current source to establish a better operating point for T5. The optimum emitter current of T5 and T6 is a compromise between a large current which increases gain and a small current which minimizes thermal drift.

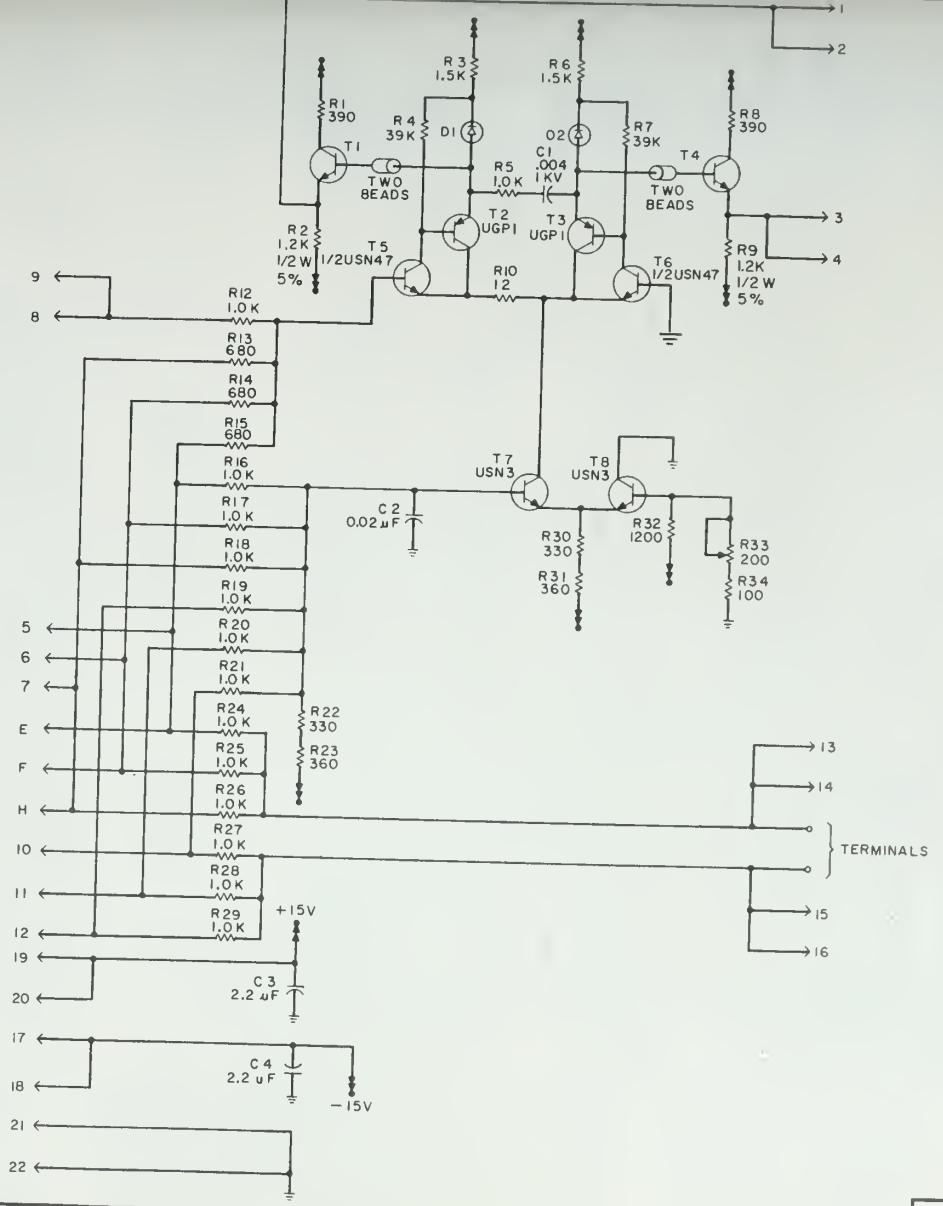
R10 reduces the open look gain slightly but shortens the settling time of the pre-amp. R5 and C1 add phrase shift necessary for

NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, 1/4 WATT, 2%.
2. UNLESS OTHERWISE SPECIFIED, DIODES ARE USZ 7.
3. UNLESS OTHERWISE SPECIFIED, TRANSISTORS ARE USN 43.
4. UNLESS OTHERWISE SPECIFIED, CAPACITANCE VALUES ARE IN MICROFARADS.
5. UNUSED PINS:

   A, B, C, O, J, K, P, R, S, T, U, V, W, X, Y, Z.

6. R12, R13, R14 MAY VARY WITH SPECIFIC APPLICATION.



TITLE	1018-280-00 DEFLECTION PRE-AMPLIFIER
DWG. NO.	D-9100-CB (CIRCUIT BOOK)
	SHEET 2 OF 3

FIGURE 15

overall system stability; the shielding beads counter a tendency toward oscillation in the output emitter followers.

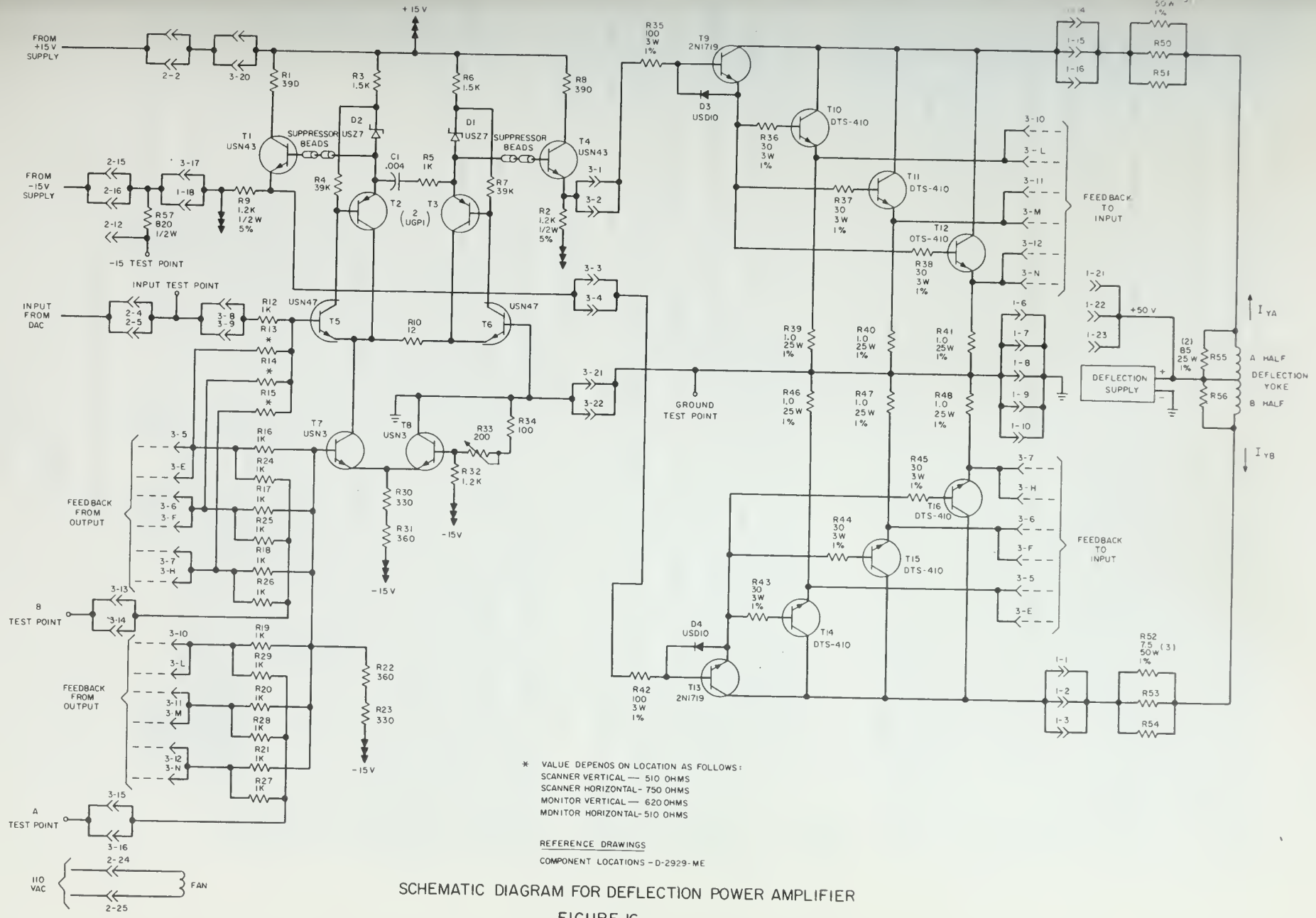
The remaining circuits on Figure 15 are part of the feedback network, shown more completely in Figure 16. The parts of the amplifier of most interest at this point are the one ohm, twenty five watt current metering resistors. These provide return signals proportional to the yoke current which is, of course, the quantity that determines spot position.

The interaction of the two feedback networks can be most easily understood from observing the sequence of events following a change in the input. A negative going signal at the input will cause the collector of T5 to rise and this will be coupled, through two emitter followers, to the base of T13. Increased current in T14, 15 and 16 will develop positive voltages across R46, 47 and 48 which are fed back to the input. Assuming that resistors are accurately matched and that amplifier gain is high, the conversion ratio of input voltage to current in the B half of of the yoke is

$$I_{YB} = V_{IN} \frac{R_{13}}{R_{12} R_{46}} \qquad \text{for } R_{13} >> R_{46}$$

Now it is inherent in the design of a differential amplifier that the rise in collector voltage of T5 will be accompanied by a similar fall in collector voltage at T6. In general, this would result in a change in current in the A half of the yoke equal and opposite to the change in the B half. Unfortunately, between the collector of T6 and the current metering resistors there are four cascaded emitters followers, all with gains dependent on temperature and other factors. Thus, it is necessary to measure current in the A half and provide appropriate feedback signals to the preamplifier.

The second of the two feedback systems not only provides for an algebraic total yoke current proportional to the input but also assures



* VALUE DEPENDS ON LOCATION AS FOLLOWS:
SCANNER VERTICAL — 510 OHMS
SCANNER HORIZONTAL — 750 OHMS
MONITOR VERTICAL — 620 OHMS
MONITOR HORIZONTAL — 510 OHMS

REFERENCE DRAWINGS

COMPONENT LOCATIONS — D-2929-ME

SCHEMATIC DIAGRAM FOR DEFLECTION POWER AMPLIFIER

FIGURE 16

that push-pull balance is maintained. This is equivalent to saying that no signal current flows in the center lead of the yoke. Since $I_{YB} + I_{YA}$ is a constant, it follows that the total of the voltages across all six metering resistors is also constant. These voltages are summed via R_{16} through R_{21} and the total compared to a value determined by R_{33}. If, for example, the total is too high, T7 conducts more heavily. This momentarily reduces both preamp output voltages although not necessarily by the same amount. Of course, the first feedback system is still effective in maintaining proportionality between input and I_{YB} so the net effect of the second feedback system is to regulate I_{YA}. The summing networks made up of R24 through R29 are used only to provide test points.

BOX 4

Essentially, the deflection amplifier in Figure 16 consists of push-pull Darlington stages which convert the pre-amp signal voltages into substantial deflection currents. The Darlington configuration provides not only the requisite power gain but also facilitates monitoring of the yoke current. Current in metering resistors R39, 40 and 41 will equal the I_{YA} yoke current except for the base current of T9, normally about one ma.

Depending on the application, yoke currents may be as large as six amperes, thus necessitating the use of parallel power transistors. Transistors used in parallel require additional testing, so much so that it is worthwhile to consider the errors that result from unmatched components. The greatly simplified circuit shown in Figure 17 will serve to illustrate the problem.

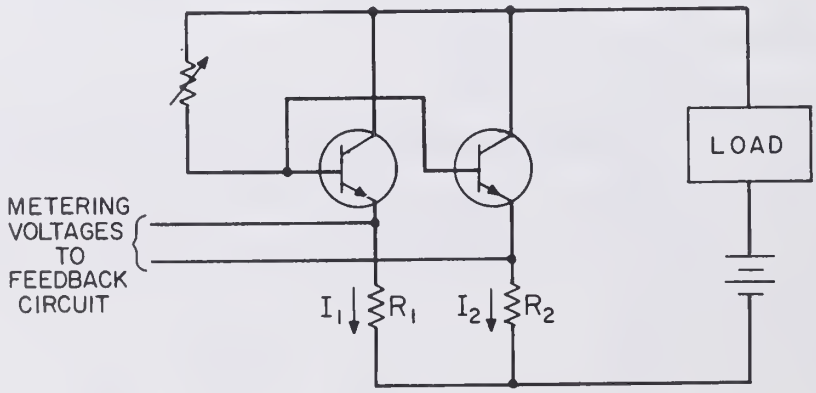


FIGURE 17

For any operating point the sum of the voltages fed back is

$$I_1R_1 + I_2R_2$$

If the total current remains constant but the division changes (as the result of a V_{BE} shift, for example) the fed back sum becomes

$$(I_1 + \Delta I)\, R_1 + (I_2 - \Delta I)\, R_2$$

or

$$I_1R_1 + I_2R_2 + [\Delta I(R_1-R_2)]$$

Obviously, the feedback circuit should respond to the total current which means the bracketed quantity should be zero.

It is important to remember that we seek a feedback signal proportional to the load current and independent of current division among the parallel transistors. It is <u>not</u> necessary that this proportionality constant be assigned with high precision. This permits relatively inexpensive power resistors to be used if they are sorted into groups of three, matched to within .1%. The matching is accomplished by connecting a large number of resistors in series with a one ampere source and measuring the drop across each with a four digit DVM.

As was previously pointed out, the voltage to current conversion ratio is determined by the input resistor R12, the feedback resistors R13 through R15 and the current metering resistors R39, 40, 41, 46, 47 and 48. All of these must be stable in order for the gain to be constant. Stability of the input and feedback resistors is simply a matter of choosing resistors with low temperature coefficients and operating them at conservative power levels. The current metering resistors, on the other hand, impose special problems because of the power that they dissipate. Each metering resistor dissipates a maximum of four watts; by using a heat-sinked 25 watt resistor the resistance change due to self-heating is minimized. The resistor heat sinks are fan-cooled and placed so that they are not "contaminated" by heat from the power transistors.

The value of one ohm was selected as a compromise between the following constraints. A large value of metering resistor helps to equalize current distribution by making V_{BE} variations less important. A large value also minimizes the error introduced by the resistance of connecting wire. (Resistors are matched to .001Ω, equivalent to a 3" length of #16 wire.) Finally, a large value increases the feedback voltage and thus minimizes the error resulting from op amp offset. On the other hand, a small value minimizes thermal drift due to self-heating.

Careful matching to make the (R_1-R_2) factor small is only part of the job. The other factor, ΔI, can be minimized by selecting sets of transistors with very similar characteristics. Each of the DTS-410 transistors to be tested is temporarily clamped to an air-cooled heat sink, power is applied and after thermal equilibrium is reached V_{BE} and I_B are recorded. The complete procedure for testing and grouping is given in Appendix III.

The Delco DTS-410 offers a number of important advantages over other transistors which were considered for this application. The device is inexpensive, has adequate voltage, current and power ratings, is rugged* and not too fast. The last qualification may seem inconsistent with our goal of maximizing deflection speed but it is not. The ultimate limitation on sweep speed is determined by the $L \frac{di}{dt}$ of the yoke and the voltage of the deflection supply. (Full scale deflection requires about 10 μsec in the Illiac III scanners.) If the deflection transistors have rise and fall times very short compared to this $L \frac{di}{dt}$ limit then the transistors "shock" the resonant circuit made up of yoke inductance and stray capacitance. The ringing that results from this shock excitation effectively increases the total deflection time. In short, the best transistor in this application is not the fastest but rather one with speed matched to the $L \frac{di}{dt}$ limitations of the yoke.

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*Units recovered from the ashes of the March 1967 fire function perfectly. No failures have occurred in use.

In amplifiers of this type it is common to place a zener diode network across the yoke to protect the driving transistors from excessive transient voltages. Such a network is not needed here due to the ruggedness of the DTS-410. It is necessary to resistively damp the yoke to improve settling time. Optimum value of the damping resistor was empirically established (using a Tektronix current probe to measure ringing in the yoke current) at 85 ohms.* On a DC basis the current in the damping resistor is only about .18% of the yoke current. Under transient conditions, however, almost the entire deflection supply voltage may appear across half of the yoke. Thus, a high wattage resistor is used to eliminate the possibility of burn out which otherwise might result from bizarre sweep patterns.

The 50 watt resistors in series with the yoke (R49 through R54, not physically part of the amplifier assembly) serve to reduce dissipation in the driving transistors. The same result could be achieved by lowering the deflection supply voltage but at the expense of increasing deflection time. In general, deflection speed is maximized by making the deflection supply voltage as large as is consistent with the voltage rating of the driving transistors.

In making precision measurements with a flying spot scanner it is customary to calibrate the overall conversion ratio (from digital representation to microns in the image plane) frequently and automatically. This calibration may be accomplished by scanning a fixed reference image or by scanning test images having easily identifiable fiducial marks. The various sources of drift in the pre amp and deflection amplifier can only

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*The value calculated from $1/2\sqrt{\frac{L}{C}}$ using the manufacturer's data for L and C is approximately 315 ohms. The discrepancy may arise from the yoke's not being a simple LC circuit.

translate the output or change the scale. Translation and magnification are easily measured in the automatic calibration process and, equally important, easily compensated for in the program. On the other hand, drift in the DAC will generally introduce nonlinearities scattered through the field, much harder to measure and much harder to compensate.

Two design goals in the Illiac III scanner have been 1), after a two hour warm up, overall system stability should be one part in 40,000 for a 30 minute period and 2), the DAC system should require readjustment not oftener than once a month to maintain 1/2 LSB linearity.

The Slit Word Group

If the image being scanned has line-like picture elements (as, for example, a bubble chamber photograph) there may be a considerable advantage in changing the flying spot scan into a flying line segment scan. The advantage can be explained in terms of additional readout information (orientation as well as position of the track) or in terms of improved signal to noise ratio.

Basically, the deformation of the CRT spot into a short line segment is possible through the use of a special diquadrupole coil mounted on the CRT. The diquadrupole has two coils (called M and N) with coil currents determining both line orientation and length. Not surprisingly, M and N are trigonometric functions of the specified angle.

Coil currents for M and N could be established by a relatively straightforward table look up process. For each digitally represented angle and length there would be stored (on a diode matrix card, for example) digital values for M and N. These would be converted to analog M and N currents through conventional DAC techniques. This approach is clean but extravagant in terms of the hardware required. In the Illiac III scanner, M and N are formed by op amp function generators. This approach permits more compact hardware but requires a few more adjustments.

Scanner logic allocates eight bits to theta, equivalent to dividing the circle into 256 parts. An angular resolution of 1.4° approaches the practical limit imposed by coil uniformity and other factors. As is indicated by Figure 1, the three most significant bits of theta specify the octant while the remaining bits specify the angle within the ortant. For the moment, our discussion will concern angles in the first octant only.

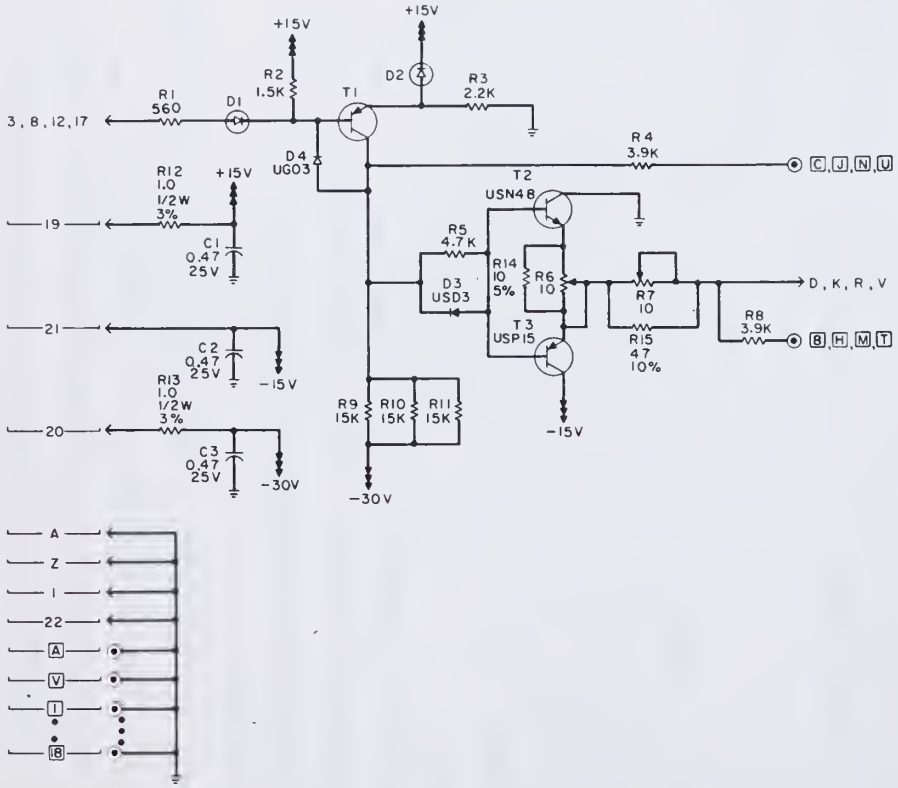
For angles in the first octant the least five theta register lines and the three "dummy" zeroes are not complemented by the complement gate (Box 7). In terms of signals to the drivers (Box 8), the angular range of 0 to 43.6° is represented by the range 0000 0000 to 1111 1000.

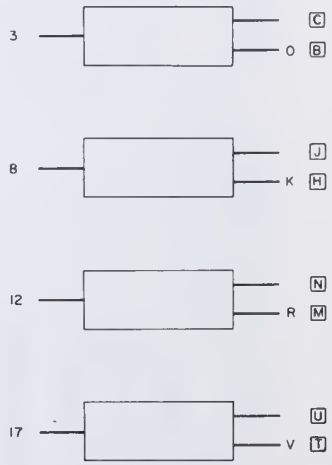
The digital to analog conversions required in the slit word group need neither high speed nor extreme accuracy. (That is, conversion speed and accuracy are not the problems here that they are in the deflection group.) Hence, it is convenient to use a simple voltage-driven ladder as the DAC. In the ladder driver shown in Figure 18, T2 and T3 constitute a SPDT switch. Depending on which of the two is saturated, the output is switched to ground or to -15 volts through an impedance of a few ohms. The eight outputs of two 1018-265-02 cards connect directly to the resistive ladder shown in Figure 19, a commercial unit built to our specifications. Unused inputs are grounded.

We now have, as the output of Box 9, an analog voltage which is proportional to theta and which can be used to generate the sine and cosine functions. A short table at this point may keep the reader from getting lost. Only enough entries are listed to give the general idea.

NOTES:

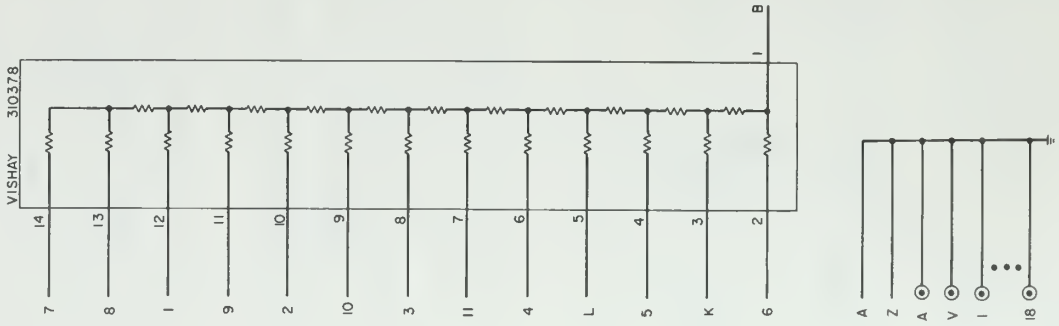
1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, 1/4WATT, 2%.
2. UNLESS OTHERWISE SPECIFIED, DIODES ARE USZ38.
3. UNLESS OTHERWISE SPECIFIED, TRANSISTORS ARE USP4.
4. UNLESS OTHERWISE SPECIFIED, CAPACITANCE VALUES ARE IN MICROFARADS.
5. TEST POINTS ARE INDICATED BY ⊙, WITH TEST PINS INDICATED BY □.
6. UNUSED PINS:
   RACK PLUG- B, C, E, F, H, J, L, M, N, P, S, T, U, W, X, Y, 2, 4, 5, 6, 7, 9, 10, 11, 13, 14, 15, 16, 18.
   TEST PLUG- O, E, F, K, L, P, R, S.





TITLE	1018-265-02 LADDER/DRIVER(4)
DWG NO.	D-8951-CB (CIRCUIT BOOK)
ISSUE 1	SHEET 2 OF 3

FIGURE 18



TITLE	1018-295-01 LADDER CARD
DWG. NO.	D-9251-CB (CIRCUIT BOOK)
ISSUE 1	SHEET 2 OF 3

FIGURE 19

Angle	0°	22.5°	43.6°
Box 6 Theta Register	0000 0000	0001 0000	00011111
Input to Box 8 (Ladder Drivers)	0000 0000	1000 0000	11111000
Output from Box 9 (Ladder)	0 Volts	-3.75 volts	-7.25 volts
Output from Box 10 (Sine)	0 Volts	4.059 volts	7.313 volts
Output from Box 11 (Cosine)	10.607 volts	9.800 volts	7.681 volts

The sine generator (shown in Figure 20) is simply an operational amplifier with nonlinear feedback. The three diodes provide a sufficiently accurate piecewise approximation to the sine function over a one octant range. Had the organization of theta been on a quadrant basis, rather than an octant basis, a much more complex diode feedback network would have been required.

The second op amp on the 307 card together with its input attenuator (R21, R22 and R23) constitutes a unity inverter. An op amp of this form (input attenuated and then restored) is easier to stabilize than the more "classic" unity inverter configuration.

The cosine generator, Figure 21, differs from the sine generator principally in that the nonlinear elements are in the input network,

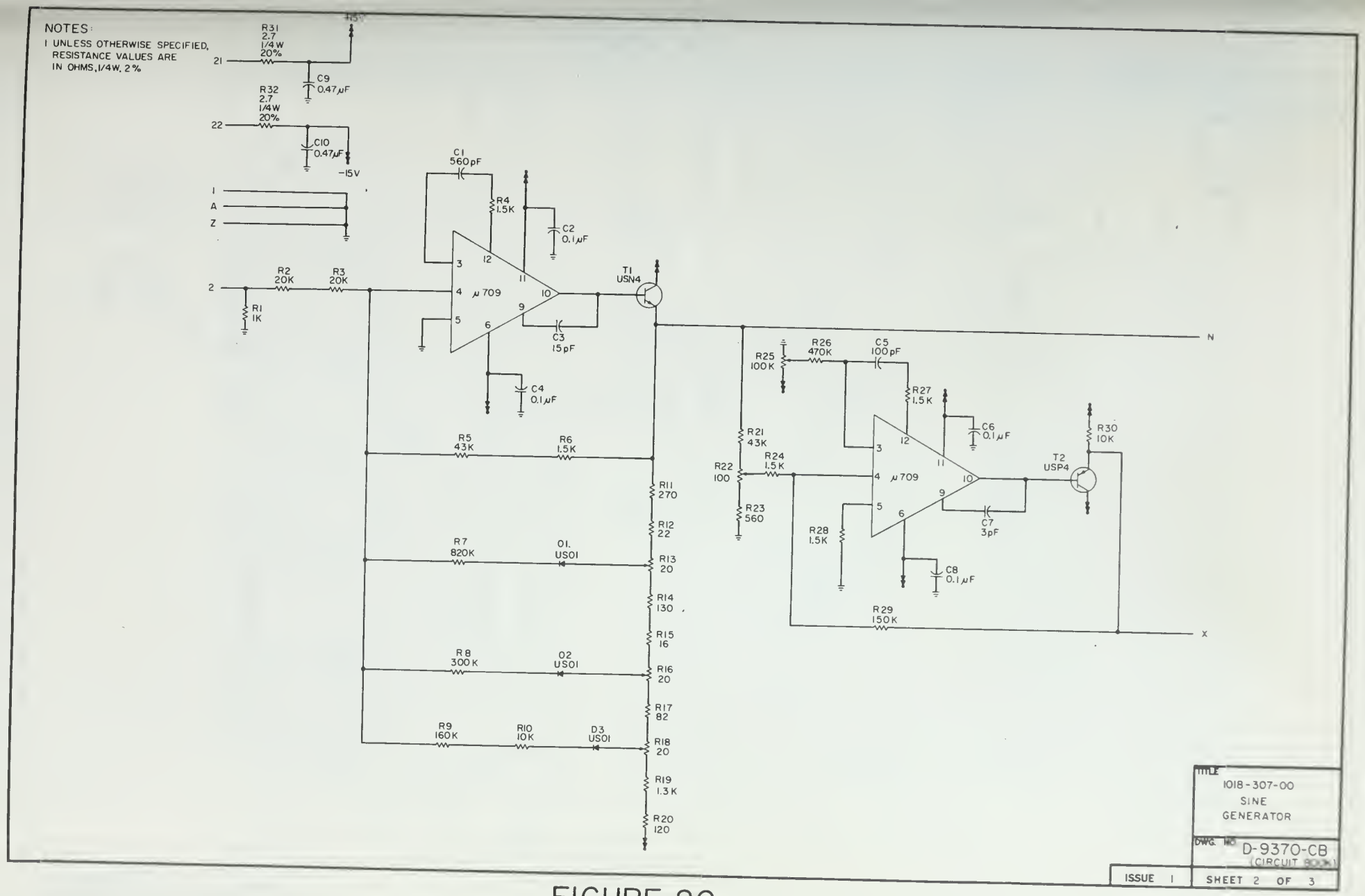
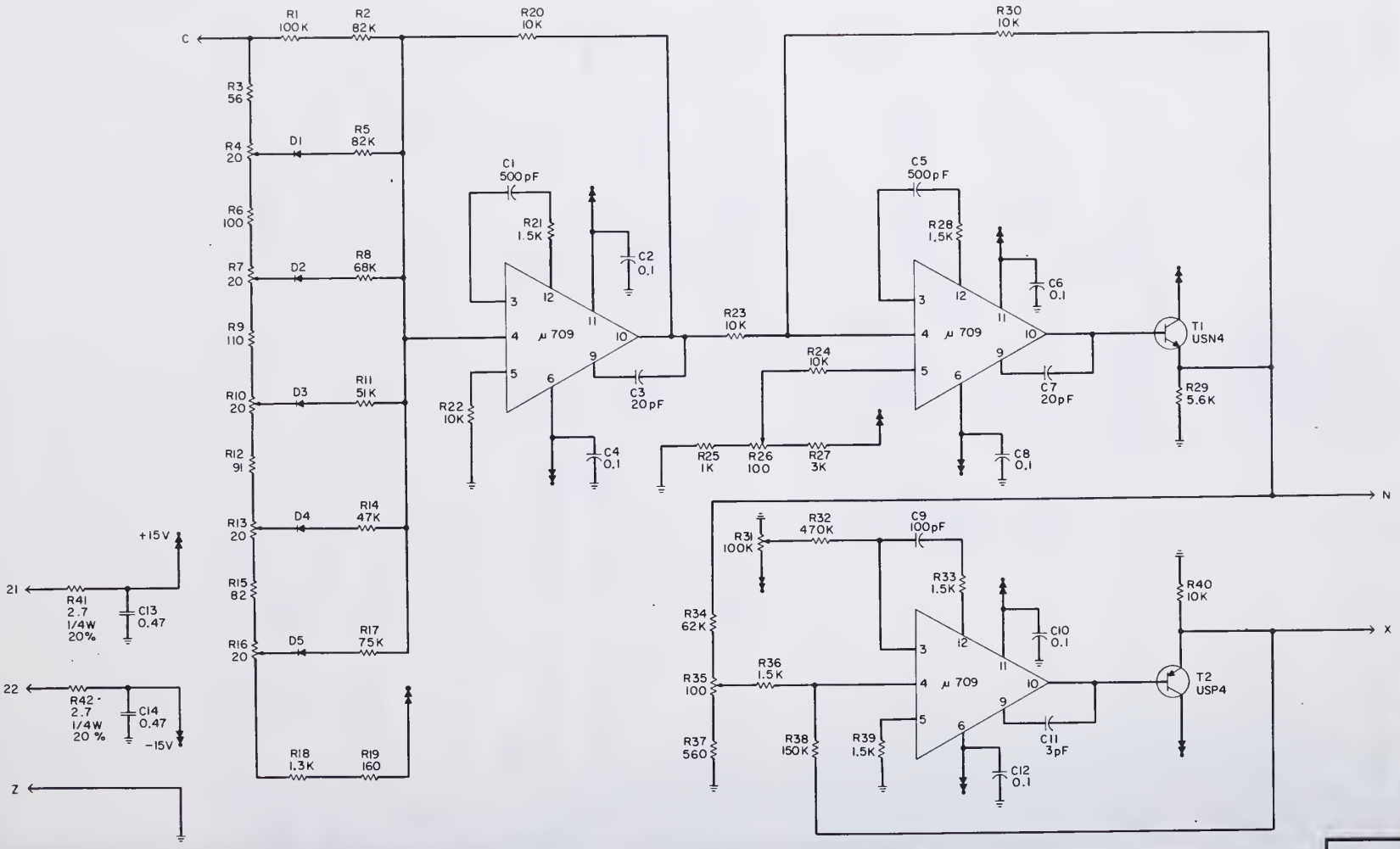

NOTES:
1 UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, 1/4W, 2%
+15V
R31 2.7 1/4W 20%
21
C9 0.47μF
R32 2.7 1/4W 20%
22
C10 0.47μF
-15V
I
A
Z
2
R1 1K
R2 20K
R3 20K
C1 560pF
R4 1.5K
C2 0.1μF
3
12
11
4
μ709
10
9
5
6
C3 15pF
C4 0.1μF
T1 USN4
N
R5 43K
R6 1.5K
R11 270
R12 22
R7 820K
01. USO1
R13 20
R14 130
R15 16
R8 300K
02 USO1
R16 20
R17 82
R9 160K
R10 10K
D3 USO1
R18 20
R19 1.3K
R20 120
R25 100K
R26 470K
C5 100pF
R27 1.5K
R21 43K
R22 100
R24 1.5K
R23 560
R28 1.5K
C6 0.1μF
C7 3pF
C8 0.1μF
R30 10K
T2 USP4
R29 150K
X
TITLE
1018-307-00
SINE
GENERATOR
DWG. NO
D-9370-CB
(CIRCUIT BOOK)
ISSUE 1
SHEET 2 OF 3

FIGURE 20

NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTANCE VALUES ARE IN OHMS, 1/4 WATT, 2%
2. CAPACITANCE VALUES ARE IN MICROFARADS
3. DIODES ARE USDI



TITLE	1018-303-00 COSINE GENERATOR
DWG. NO.	D-9330-CB (CIRCUIT BOOK)
ISSUE 1	SHEET 2 OF 3

FIGURE 21

not in the feedback. Over the range 0 to 45° the cosine function has greater curvature than the sine function; to obtain the same accuracy from a diode break network more break points are required for the cosine. The nonlinear network of the sine generator has three diodes, that of the cosine generator, five.

Having the nonlinear network of the cosine generator on the input leads to an unfortunate complication. The difficulty is more aesthetic than practical but will be mentioned here so the author cannot be charged with evasiveness.

The input impedance of the cosine generator is not constant but ranges from about 1925 ohms to 1805 ohms as a function of the input voltage. If the card were driven from a low impedance source, this 6.5% variation in input impedance would be of no consequence. The source is, however, a resistive ladder with a Thevenin equivalent impedance of 1K. Thus, the voltage at the input of the cosine generator is not strictly proportional to theta but is "distorted" by the variable loading of the input network. Worse, since the sine and cosine generators are both tied to the ladder, the "distortion" caused by the cosine generator appears in the sine generator output.

We could, of course, interpose an additional op amp between the ladder and its two loads. Alternatively, a dummy diode network could be added with its only function being maintenance of constant input impedance. Neither step is needed. When the constant load of the sine generator is added to that of the cosine generator, the total load seen by the ladder varies only about 3.3% or one LSB. Since both generators are generously provided with adjustment resistors (necessitated principally by diode variations) it is simply a matter of adjusting the complete system for the correct transfer functions. Using a ladder as the source, and with both generators as loads, the cosine card is adjusted followed by the sine card.

We have, at this point, positive and negative sine and cosine functions for a very restricted range of angles. A couple of simple tricks will permit us to use these two humble function generators over the entire circle. We begin by defining M and N for each of the octants.

OCTANT	M	N
000	cos θ	sin θ
001	sin(π/4-θ)	cos(π/4-θ)
010	-sin θ	cos θ
011	-cos(π/4-θ)	sin(π/4-θ)
100	-cos θ	-sin θ
101	-sin(π/4-θ)	-cos(π4-θ)
110	sin θ	-cos θ
111	cos(π/4-θ)	-sin(π/4-θ)

In the table above, "θ" refers to the least significant five bits of the theta register.

Two techniques are needed to make this system work: 1), a method of selecting either θ or (π/4-θ) as the input to Box 8 and 2), a method of switching analog signals between function generators and amplifiers.

The (π/4-θ) function is achieved easily by gating the complement of the least significant five bits of theta to the ladder drivers, Box 8. By itself, this operation would introduce an error of a unit in the least significant digit. Rather than correcting this by adding a unit in the least place (which could require a five digit adder) it is simpler to add dummy stages to the theta register. These dummy stages (always zero)

are complemented along with theta and reduce the complementary error to 1/8 LSB. This requires no extra driver cards since each 1018-265-02 has four ladder driver circuits. Fortunately, within any octant the function is θ or $(\pi/4-\theta)$ for both M and N.

The function selector shown in Figure 22 simply provides a path between a function generator and an amplifier, the particular analog path being specified by the logic inputs. If, for example, T1 is cut off and T2, T3 and T4 are saturated, the analog signal present on pin 2 appears at the output (inverted) and the other three analog signals are suppressed. The suppression afforded by heavily saturated germanium transistors is more than adequate for this application. Note that two different input circuits are needed for switching; the NPN circuits are used for +cosine and +sine, the PNP circuits for the negative functions.

BOX 13

The M and N attenuators of box 13 are adaptations of an ingenious design by Professor Kenneth C. Smith and Mr. A. Sedra of the University of Toronto. For the circuit shown in Figure 23 the following relations obtain

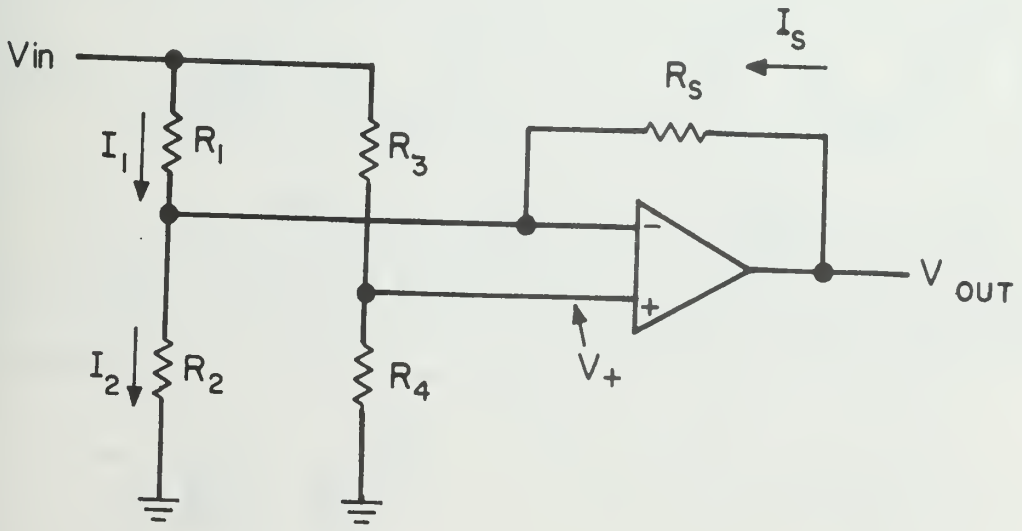
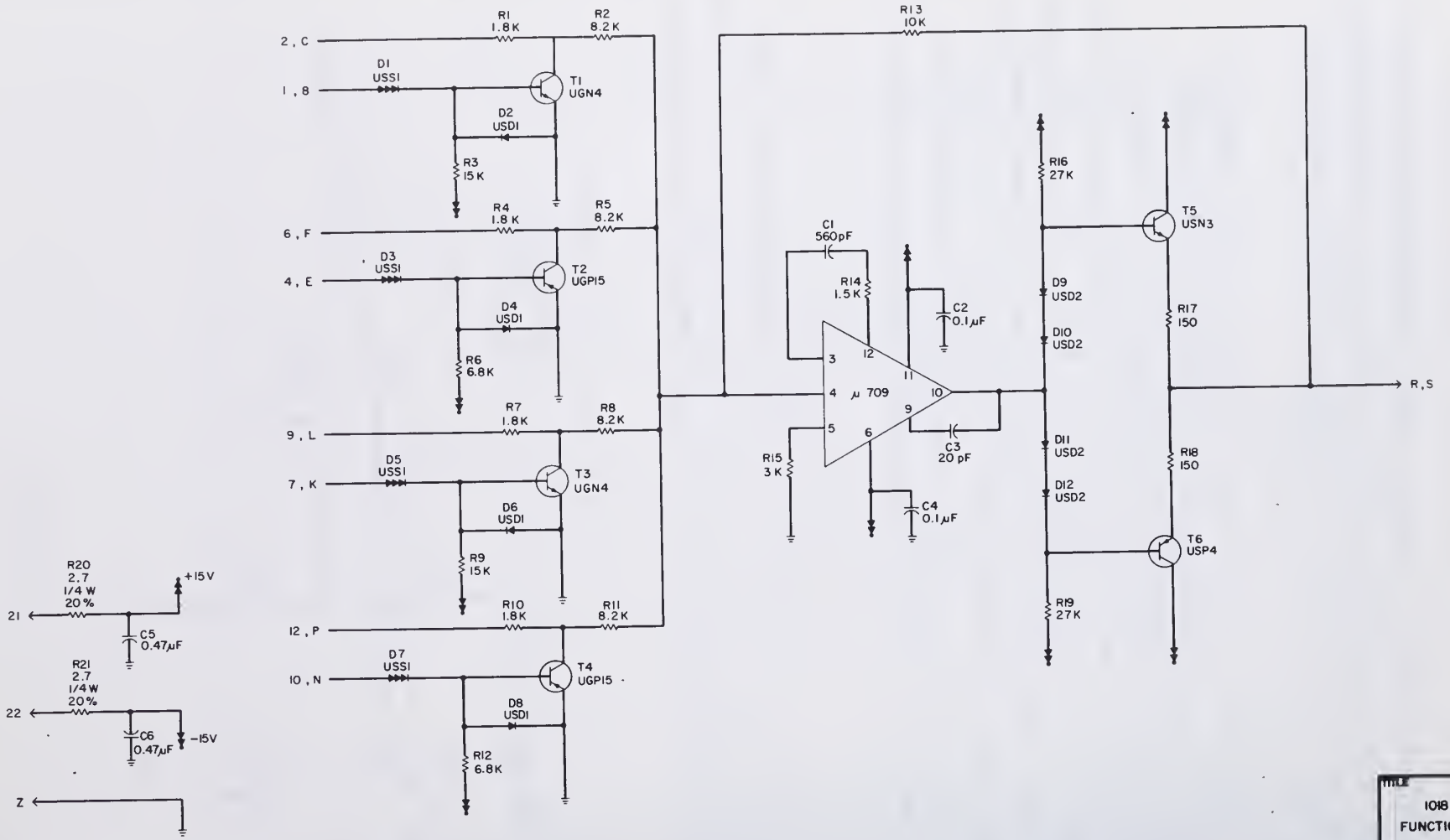


FIGURE 23

NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, 1/4 WATT, 2%.



TITLE	1018-309-00 FUNCTION SELECTOR
DWG. NO.	D-9390-CB (CIRCUIT BOOK)
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FIGURE 22

$$V_- = V_+ = V_{IN} \frac{R_4}{(R_3 + R_4)}$$

$$I_1 = \frac{V_{IN} - V_-}{R_1} = V_{IN} \left[\frac{R_3}{R_1(R_3 + R_4)} \right]$$

$$I_2 = \frac{V_-}{R_2} = V_{IN} \left[\frac{R_4}{R_2(R_3 + R_4)} \right]$$

$$I_5 = I_2 - I_1 = V_{IN} \left[\frac{R_1R_4 - R_2R_3}{R_1R_2(R_3 + R_4)} \right]$$

$$V_{OUT} = V_- + I_5R_5$$

$$V_{OUT} = V_{IN} \left[\frac{R_4}{(R_3 + R_4)} + \frac{R_5(R_1R_4 - R_2R_3)}{R_1R_2(R_3 + R_4)} \right]$$

$$V_{OUT} = V_{IN} \left[\frac{R_1R_2R_4 + R_5(R_1R_4 - R_2R_3)}{R_1R_2(R_3 + R_4)} \right]$$

$$V_{OUT} = V_{IN} \left[\frac{R_2(R_1R_4 - R_3R_5) + R_1R_4R_5}{R_1R_2(R_3 + R_4)} \right]$$

if $R_1R_4 = R_3R_5$ this simplifies to

$$V_{OUT} = V_{IN} \left[\frac{R_4R_5}{R_2(R_3 + R_4)} \right]$$

The circuit so simplified has a very attractive property, namely, the gain is inversely proportional to a resistor (R2) one end of which is grounded. Since one end of R2 is grounded, it can be replaced by a network of the form shown in Figure 24.

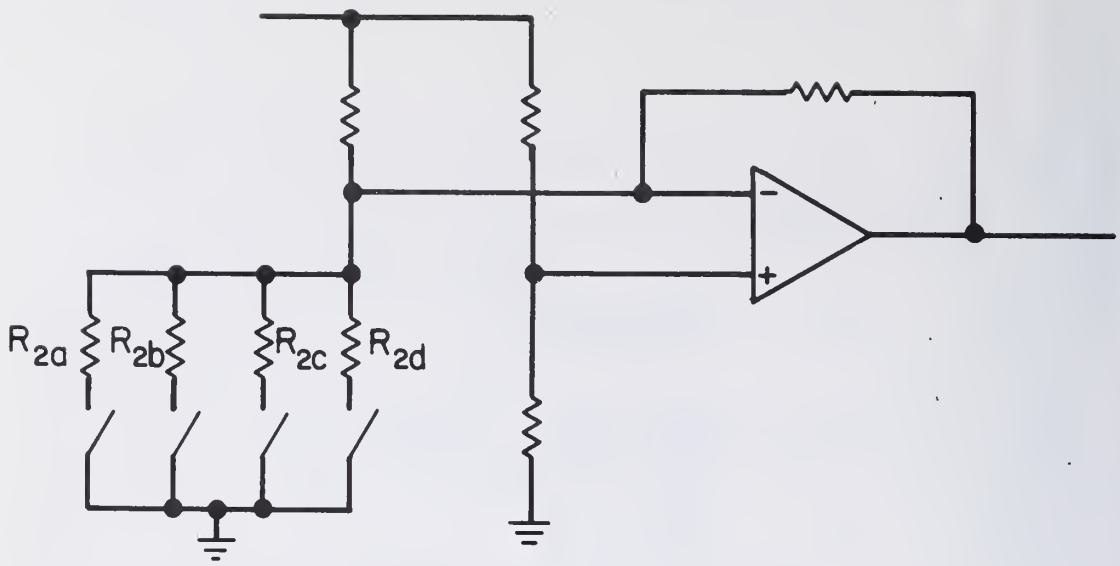

FIGURE 24

Since only R_2 varies in the circuit above, the gain may be expressed as $G = K/R_2$. For resistors R_{2a} and R_{2b} the associated gains would be K/R_{2a} and K/R_{2b} respectively. If <u>both</u> R_{2a} and R_{2b} are switched in, the gain is determined by this parallel resistance

$$\frac{1}{\frac{1}{R_{2a}} + \frac{1}{R_{2b}}}$$

Thus, the gain with two resistors is

$$K(1/R_{2a} + 1/R_{2b})$$

or exactly equal to the <u>sum</u> of the gains resulting from those resistors considered separately. By choosing N different R_2 resistors with binary weights we create an amplifier whose gain can be set at any of 2^N values.

The attenuator configuration appropriate to this application is shown in Figure 25. If R34 is momentarily assumed to be zero, the gain with T1 conducting is

$$\frac{3000 \cdot 3000}{4000(12000 + 3000)} = .15$$

NOTES: UNLESS OTHERWISE SPECIFIED —
1. RESISTANCE VALUES ARE IN OHMS, 1/4 WATT, 2%
2. DIODES ARE USD1.
3. TRANSISTORS ARE UGN4

* 1/4 W, 2% SELECTED TO BE ± 1/2 % ACCURATE

108-312-00
ATTENUATOR

D-94420-CB
(CIRCUIT BOARD)

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FIGURE 25

Naturally, the gain with only T2 conducting is half this value and so on for the remaining switches.

The input impedance due to resistors R36 and R33 is a constant 15K if we assume the loading due to terminal 5 of the op amp to be negligible. The impedance of the branch consisting of R35 and the gain-controlling resistor (or resistors) is <u>also</u> 15K since the op amp ensures that the voltages across R35 and R36 will be equal. With the input impedance totally independent of the gain-controlling resistance, the addition of a small resistor at R34 simply lowers the gain by a fixed ratio. For the values specified, gain with T1 conducting is

$$\frac{7500}{470 + 7500} \quad (.15) = \quad .1415,$$

the value required to match the function generator output range to the amplifier input range.

A crucial requirement of the switched-gain amplifier is that it works with both polarities of input signals. In other words, the switch transistors must be cut off or saturated depending on the logic input but independent of the collector voltage polarity. Assuring saturation is not a problem for either polarity. Cutoff, on the other hand, is potentially a problem for negative collector voltages. The problem is solved by reverse biasing the switch transistors so that for the most negative collector voltage the collector-base junction is still reverse biased.

Eight switch transistors permit 256 different values of gain to be specified on the 1018-312-00 card. In practice, only a few of these are used; the inclusion of three logic diodes for each switch facilitates this selection.

The amplifiers (box 14) and diquadrupole coil (box 15) are both commercially obtained. Specifications for them are summarized in Appendix IV.

The Correction Group

The correction group embraces the various circuits used to compensate for geometric distortion within the CRT. For convenience, the defocus circuitry (which provides controlled spot size degradation) is also included here.

Dynamic Focus Correction

For a flat faced CRT the total beam length can be shown to be approximately

$$L = K_1 + K_2(X^2 + Y^2)$$

where X and Y represent deflections relative to center screen. There is little merit in deriving functions of greater exactness since some of the relevant factors such as field distribution within the deflection yoke are nearly unmeasurable. If we allow the preceding equation as a satisfactory approximation it then follows that the field required for focusing is

$$B_{focus} = B_{static} + K(X^2 + Y^2)$$

where B_{static} represents the focus field for an undeflected spot and $K(X^2 + Y^2)$ represents the dynamic focus correction. The general system for generating the composite focus field is shown in Figure 26.

The X and Y inputs for Figure 26 are taken from the X and Y DAC outputs and represent voltages in the range 0 to -8.190 volts. These voltages are shifted by +4.095 volts (so that zero voltage corresponds to zero deflection), rectified, squared and summed using conventional op amp techniques. After attenuation by the appropriate factor, the dynamic focus correction signal is amplified by a commercial amplifier of conventional design.

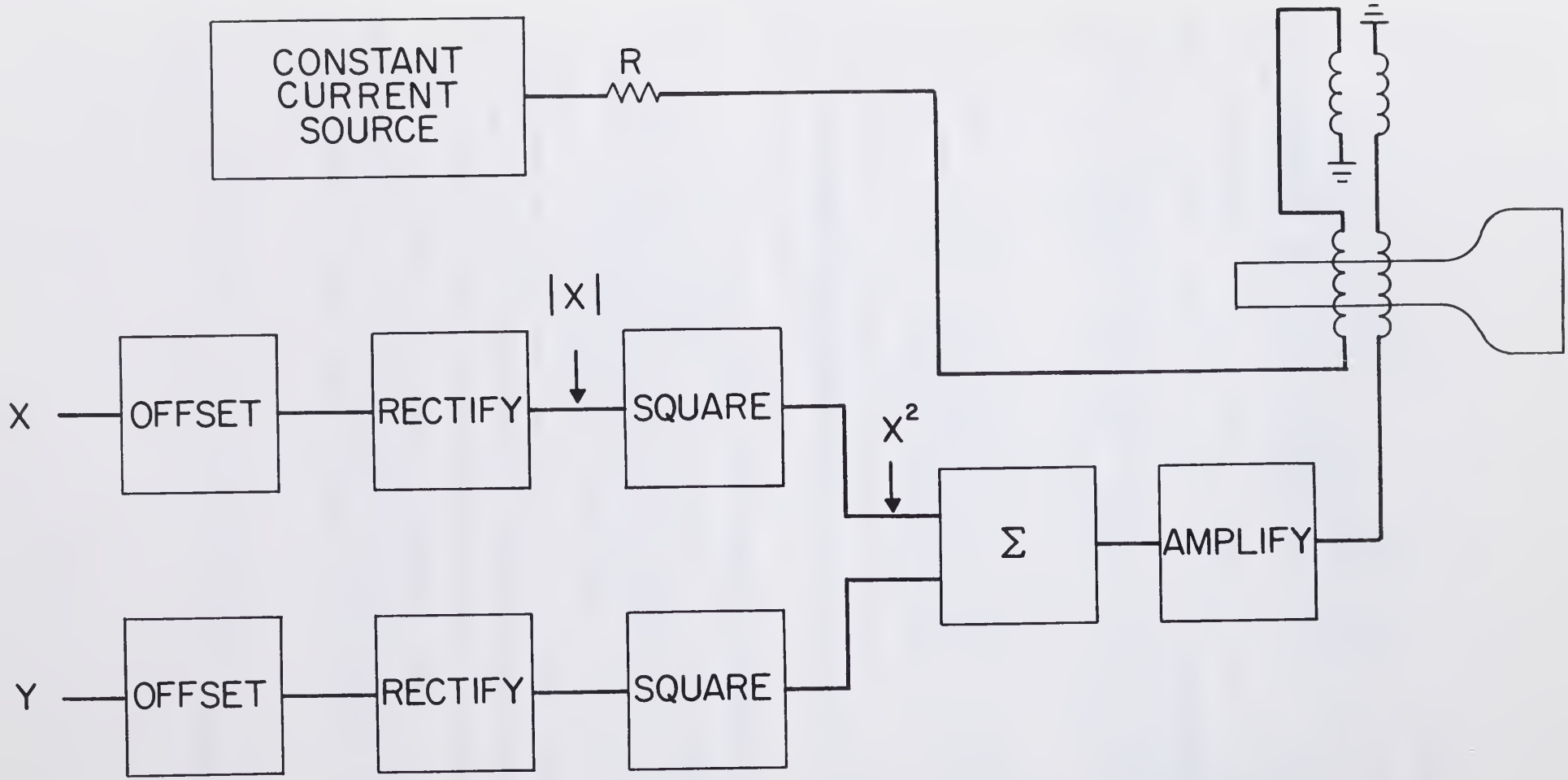

CONSTANT CURRENT SOURCE
R
|X|
X
OFFSET
RECTIFY
SQUARE
X²
Σ
AMPLIFY
Y
OFFSET
RECTIFY
SQUARE

FIGURE 26

As Figure 26 implies, the static and dynamic focus fields are obtained through separate windings on the focus coil assembly. This is chiefly a matter of efficient design. Since the static focus current by definition does not change, the static winding can have relatively high inductance. This permits a large number of turns on the static winding and thus reduces the current drawn from the constant current source.

On the other hand, the dynamic focus winding needs low inductance to accommodate rapid sweeps. The smaller number of turns implied by low inductance poses no problem as the B contribution required for the dynamic winding is at most about 5% of the static field.

Unfortunately, the two focus windings are coupled with the result that current changes in the dynamic winding induce voltages in the static winding. This would be of no consequence if the static coil could be supplied from a perfect current source. Most laboratory power supplies operated as current supplies fall short of perfection. They usually have a permanently connected large output capacitor which means that transiently, the supply is a voltage source. The effective source impedance can, of course, be increased by adding a series resistor R. This approach is limited by the amount of power one is willing to waste in the series resistor.

Another more effective (and more expensive) technique is to use a second focus coil assembly to cancel the induced voltage. This approach is particularly attractive if the focus correction circuits alternately service two CRT's. Both coil assemblies are mounted in the usual way; the coil on the idle CRT serves as the voltage cancellation dummy. This requires relays or similar devices to switch coil orientation at the time a CRT is selected.

Defocus

In picture processing, the smallest spot diameter does not necessarily yield the most useful data. At times, simple but useful preprocessing is achieved by merely enlarging the spot (or the thickness of the slit) until it corresponds more nearly to features in the picture. The conversion from the two bit line-width register to an analog defocusing voltage is shown in Figure 27.

Note first that only three of the line register states need be decoded, the 00 state being defined as maximally sharp focus. These three signals (group A in Figure 27) are then encoded into three eight bit words in the 240-00 card. Finally, the eight logic outputs of the 240-00 are converted to an analog voltage in the 1018-301-01 card, a simple current summing DAC card shown in Figure 28.

The wiring between group A and group B can be specified so that each of the three active line register states selects one of 255 defocusing levels. This arbitrary assignment of defocus levels is necessary since various classes of picture processing may require different defocusing levels. The connection pattern from A to B is established by a printed circuit card so it may be changed easily.

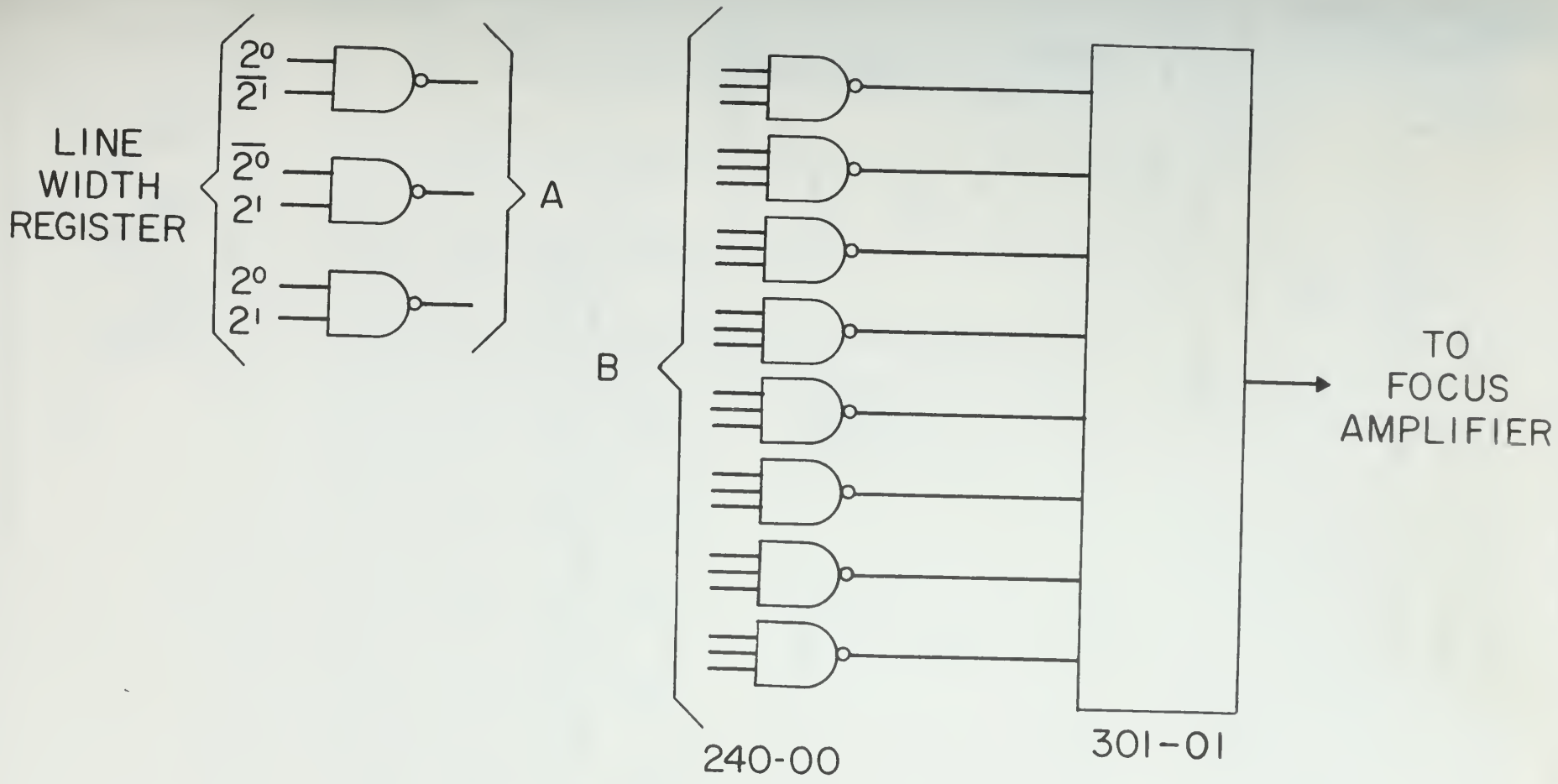
Pincushion Correction

Inherent in any flat faced CRT is geometric distortion called pincushion. The name stems from the fact that a rectangular raster of deflection currents produces a figure with pointed corners and bowed-in sides. This distortion is approximated by the functions

$$X = k_1 I_x (1 + k_2 (I_x^2 + I_y^2))$$

$$Y = k_1 I_y (1 + k_2 (I_x^2 + I_y^2))$$

where X and Y represent actual deflections and I_x and I_y are the deflecting currents. As was true with dynamic focus correction, expressions involving



DEFOCUS SYSTEM

FIGURE 27

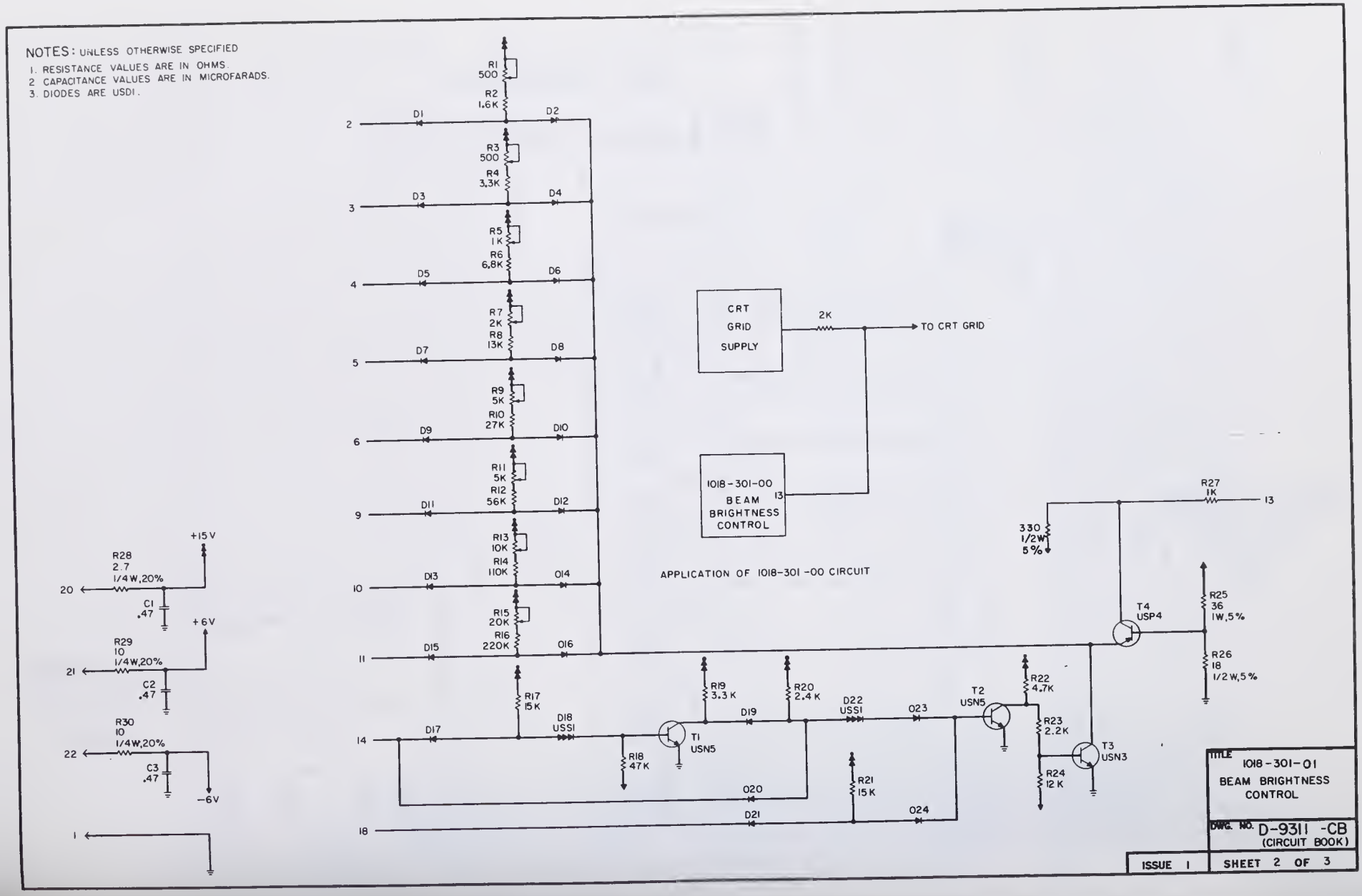

NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTANCE VALUES ARE IN OHMS.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. DIODES ARE USDI.
R1 500
R2 1.6K
D1
D2
R3 500
R4 3.3K
D3
D4
R5 1K
R6 6.8K
D5
D6
R7 2K
R8 13K
D7
D8
R9 5K
R10 27K
D9
D10
R11 5K
R12 56K
D11
D12
R13 10K
R14 110K
D13
D14
R15 20K
R16 220K
D15
D16
R17 15K
D17
D18 USSI
R18 47K
T1 USN5
R19 3.3K
D19
R20 2.4K
D22 USSI
D23
T2 USN5
R22 4.7K
R23 2.2K
R24 12K
T3 USN3
R21 15K
D20
D21
D24
CRT GRID SUPPLY
2K
TO CRT GRID
1018-301-00 BEAM BRIGHTNESS CONTROL
13
APPLICATION OF 1018-301-00 CIRCUIT
R27 1K
13
330 1/2W 5%
T4 USP4
R25 36 1W,5%
R26 18 1/2W,5%
+15V
R28 2.7 1/4W,20%
20
C1 .47
+6V
R29 10 1/4W,20%
21
C2 .47
R30 10 1/4W,20%
22
C3 .47
-6V
1
2
3
4
5
6
9
10
11
14
18
TITLE
1018-301-01
BEAM BRIGHTNESS CONTROL
DWG. NO. D-9311-CB
(CIRCUIT BOOK)
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FIGURE 28

higher powers of $(I_x^2 + I_y^2)$ are not necessarily more accurate owing to inhomogeneities in the yoke, imperfect gun alignment and other factors.

There are a number of ways of reducing pincushion distortion. Simplest of these is the addition of a special pincushion corrector assembly near the bell of the CRT. This may be either a ring of permanent magnets or a series of coils which introduces a compensating field distortion. Pincushion correctors of this type are satisfactory in many applications but are not useful in precision scanners because of the spot size degradation they necessarily introduce.

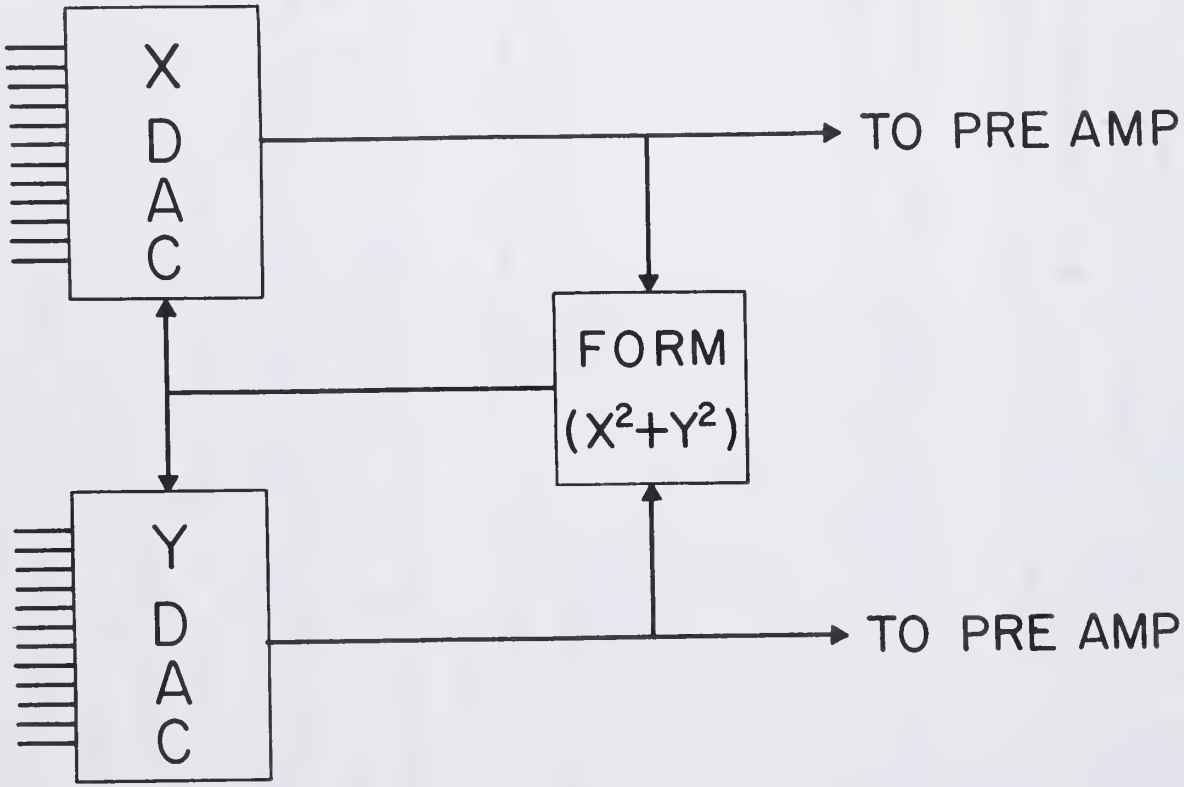
Pincushion distortion can also be reduced by digitally transforming the deflection coordinates before they are sent to the DAC units. The transformations are of the form

$$X' = X(1 - k(X^2 + Y^2))$$
$$Y' = Y(1 - k(X^2 + Y^2))$$

where the primed variables represent the coordinates after transformation. This approach can cancel at least 90% of the distortion but requires a substantial investment in hardware.

A very similar technique might be called digital post-correction. Here, whenever the true coordinates of a picture element are needed, the DAC coordinates are multiplied by a corrective polynomial. This polynomial can cancel optical distortions in the image as well as the pincushion distortion. The Illiac III scanners use digital post-correction.

An analog system for pincushion reduction is shown in Figure 29. The circuits used to generate $(X^2 + Y^2)$ need not be discussed since they are, in fact, the same circuits used for focus correction (Figure 26). What <u>is</u> new in Figure 29 is the addition of an analog input to each DAC unit.



ANALOG PINCUSHION CORRECTION

FIGURE 29

A moment's reflection will convince the reader that multiplication is intrinsic to nearly any DAC system. That is to say, over some range the analog output is the product of the digital input and the reference voltage. In Figure 29 the correction function $(X^2 + Y^2)$ simply modulates the DAC reference voltage over a range of about five percent. The two feedback loops do not pose an oscillation hazard because of the very low loop gains.

Analog pincushion correction is not suitable for a precision scanner since the nonlinear devices needed to generate X^2 and Y^2 have temperature coefficients that would degrade long term stability. Where very high position accuracy and repeatability are less important (as in large screen monitors) the analog correction scheme has merit. Large screen cathode ray tubes often have spherical faces but correction is still required since the sphere of the face is not concentric with the center of the deflection yoke.

The CRT Brightness Group

Establishing the proper level of beam current in the CRT is, by all odds, the most nerve-racking procedure in the entire lexicon of scanner adjustments. Too little beam current and you have poor signal to noise ratio; too much beam current and you destroy a very expensive piece of hardware. It is not overly dramatic to say that any useful operating point is uncomfortably close to disaster.

There are several reasons why phosphor damage is a much more serious hazard in a flying spot scanner than in, say, a television set. For one thing, the phosphor in a flying spot CRT must have a very short persistence so that the opacity information of a particular picture element is not "contaminated" by previously scanned areas. If one insists on sub-microsecond persistence, the choice is limited to P16, a phosphor very easily damaged by excessive beam currents.

Drift in the CRT characteristics can easily trap the unwary. Our experience has been that from a cold start, the grid voltage needed to

obtain one μA of beam current may drift several volts in eight hours. (The significance of this enormous change will be demonstrated shortly.) On the advice of the manufacturer, we now leave the CRT filaments hot around the clock. Drift, though still present, is a less serious factor after a few weeks of continuous filament energization.

Probably the most serious hazard to the phosphor comes from what might be called program dependent effects. For a given beam current it makes a great deal of difference as to whether the entire field or some tiny portion of the field is scanned. In the latter instance, a particle of phosphor may not have time to cool off before being reexcited, a situation leading to destructively high temperatures. As yet, there is no complete and general solution to this problem. The solution used in the Illiac III scanner is to program the beam current level at the time the scanning pattern is established.

The first step in establishing a reasonable operating point is to devise a means of measuring the beam current. A sensitive taut band meter in the second anode lead will give useful if not extremely accurate readings. A few observations are appropriate. One, the first concern in metering a high voltage circuit should be to minimize the likelihood of electrocution. Two, it may be necessary to shield the meter with a high voltage screen to eliminate errors due to electrostatic forces. Three, the smallest current which can be read with any accuracy will be about 1 μA. Four, the leakage resistance of all associated wiring, etc. should be very high (greater than 10^{11} ohms).

A more convenient measurement point is in the cathode lead of the CRT. The manufacturer states that for currents less than about 5 μA essentially all of the cathode current reaches the screen. In our scanners a precision one megohm resistor in the cathode lead is monitored with a digital voltmeter. Cathode to filament "leakage" (actually not an ohmic leakage) is minimized by biasing the filament twelve volts positive with respect to the cathode. This is equivalent to reverse biasing the filament-

cathode diode. This system works well as long as no important leakages develop within the CRT. Our luck has been only fair in this respect.

Neither method of measuring beam current can be trusted for currents much less than 1 μA. Yet, it will be demonstrated shortly, many scan patterns require that beam currents be in the nanoampere range. We circumvent the difficulty by measuring the beam current vs. bias characteristics of the CRT using the following procedure.

1) Establish a raster over the entire field. Decrease bias until 1 μA beam current is measured either in the cathode or anode lead of the CRT.

2) Monitor the output of a photomultiplier tube (PMT) which receives light from the CRT. Increase the high voltage supplied to the PMT until the output is maximum suggested by PMT data sheet. (For RCA 8575 this is 200 μA.)

3) Increase bias by ΔV, record PMT output.

4) Repeat step 3 until PMT output drops to less than 10% of starting value. At that time increase the PMT supply voltage to increase PMT sensitivity by a factor of ten.

5) Continue in this fashion until PMT output is obscured by dark current.

With this technique it is possible to obtain a smooth plot of current vs bias over a five decade range (see Figure 30). We have assumed that beam current and light output are proportional, a reasonable assumption for currents much below the saturation level of the phosphor.

To establish a beam current of (for example) 1 nA, one measures the bias necessary to obtain 1 μA (using a full field scan to prevent phosphor damage) and then biases the CRT an extra 7.3 volts. The previously discussed drift makes it necessary to establish the 1 μA bias point at least daily.

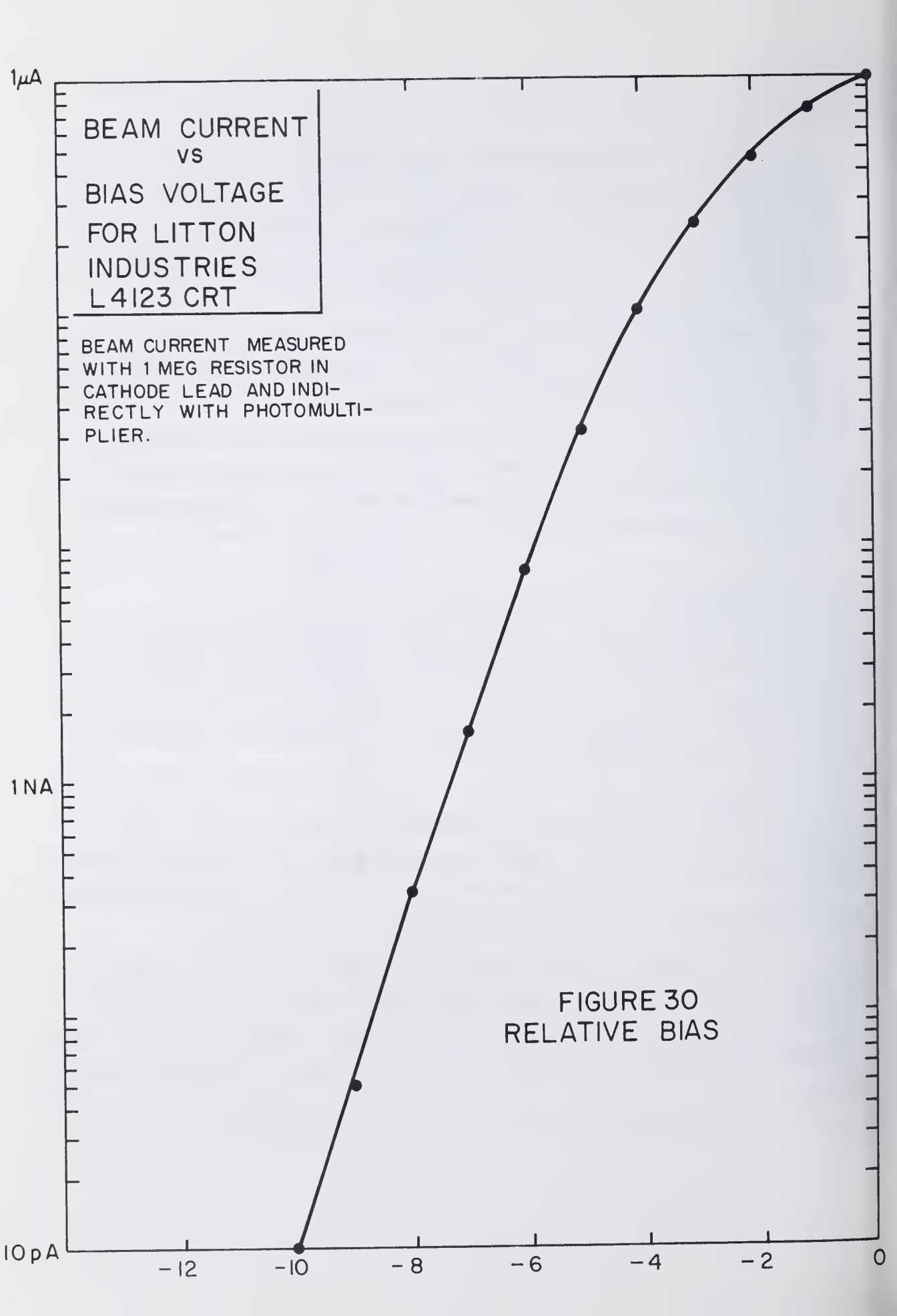


FIGURE 30
RELATIVE BIAS

Limitations on CRT Beam Current

There are two totally independent mechanisms which limit allowable beam current in a CRT. The first of these is the thermal limitation. Most of the energy in an electron beam produces heat, which is dissipated principally by conduction through the faceplate glass. If the temperature rise of the phosphor exceeds about 600°C, phosphor material is vaporized with attendant irreversible loss in light output. A simple example illustrates the extent of this problem. If a 1 μA beam is accelerated through 20 KV and produces a spot .001" in diameter, the power density at that spot will be about 25,000 watts/in^2.

The relation of temperature rise to the many beam parameters is extremely complex. Elliot* investigated the problem in considerable detail and derived the relation

$$\Delta T = \frac{1.3 \times 10^{7} \, I \, t^{7/8}}{A V^{1/2}}$$

where ΔT = temperature rise in °C

I = beam current in amperes

V = accelerating voltage in kilovolts

A = beam area in cm^2

t = time, in seconds, that the beam remains in one position.

This equation results from making important simplifications upon a mathematically unmanageable three dimensional heat-flow problem. It is intended to be accurate only for short pulses (less than about 320 μsec. in our application) and does not consider the effects of beam motion.

More important, the equation gives the temperature rise caused by a single pulse, isolated in time. Obviously, if the same area is pulsed at a repetition interval less than the cooling time there will be a

*W. R. Elliot, "Limitations on High Energy Cathode Ray Tube Beams with Regard to Phosphor Life", 6th National Symposium, Society for Information Display.

cumulative heat build up. Equations are given for calculating the cooling period but, again, the mathematical model is not applicable to scan patterns involving varying degrees of overlap and other non-simple behavior. In any case, beam current is more severely limited by total charge effects.

Pfahnl* shows in his paper that the light output of a CRT decreases as a simple function of the total charge transferred to the phosphor. The deterioration depends neither on accelerating voltage nor on the rate at which change is accumulated. (Naturally, charge-induced deterioration is in addition to any thermal destruction of the phosphor.) The charge required to reduce light output by one half varies greatly from one phosphor type to another; unfortunately, the charge constant for P16 is extremely low, .1 coulombs/cm^2. For a .001" diameter spot and 1 μA beam current this means that the beam can illuminate a given area only about .5 seconds integrated over the entire life of the CRT. Of course, if such a beam paused for .5 seconds in one location the phosphor then would be destroyed by thermal effects.

Two extremes of operation will help to establish safe levels of beam current. As the first example, consider a scan pattern which distributes the beam uniformly over the entire 60 x 90 mm field. A beam current of 2 μA would transfer 5.4 coulombs (equal to .1 coulomb/cm^2) in only 750 hours. Thus, it seems clear that beam currents should be held below this value since, in general, beam positions are not uniformly distributed over the field. (Areas with fiducial marks are typically scanned more frequently than other regions.) If the total charge is unevenly distributed over the field then some area will wear out long before 750 hours has elapsed.

At the other extreme, it may be necessary to leave the beam in one location for an extended time in order to adjust the CRT focus and

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*A. Pfahnl, "Aging of Electronic Phosphors in Cathode Ray Tubes", Bell Telephone Laboratories Monograph 3989.

deflection system. For an observation period of 15 minutes, beam current should be reduced to much less than 500 pA to avoid damage. Good practice dictates that the beam be defocused wherever possible during such adjustment runs.

The beam brightness circuits (box 22) shown in Figure 31 combine two functions on a single card. The eight logic level inputs (pins 2,3,4,5, 6,9,10,11) simply divert binary-weighted currents so that the emitter current of T4 varies from 0 to 12.75 ma in increments of .05 ma. If we ignore the base current of T4 momentarily, we see that this current modulates the grid voltage over a range of 25.5 volts in .1 volt steps. The nonzero base current is no problem since R1, R3, etc. are adjusted for the proper grid swing. The long string of zener diodes in the collector of T4 simply reduces the power dissipated in T4.

Pin 14 on the 301-00 card is the input to the phosphor protection circuit. A positive logic-level transition on pin 14 causes T2 to conduct momentarily because of the delay through T1. If positive transitions occur at least every 3 μsec then T2 will be saturated, T3 will be cut off and the current summing mechanism will be enabled. Whenever there is no signal change at pin 14, T3 saturates, forcing the CRT grid to its most negative level. The 3 μsec "on" time can be doubled by adding .1 μF from the base of T2 to ground. Pin 18 provides a DC override of the protection system.

The Detection and Signal Conditioning Group

Of all light detecting devices, only the photomultiplier has the high sensitivity needed to measure the tiny light output of one CRT. Very high sensitivites are easily obtained but this is only part of the problem. Consider the following. When operated at 2000 volts, the RCA 8575 photomultiplier has a typical current gain of 4×10^6. An output current of 200 μA (the largest recommended anode current) then implies a cathode current of 5×10^{-11} amperes or about 300 electrons/μsec. The output pulse

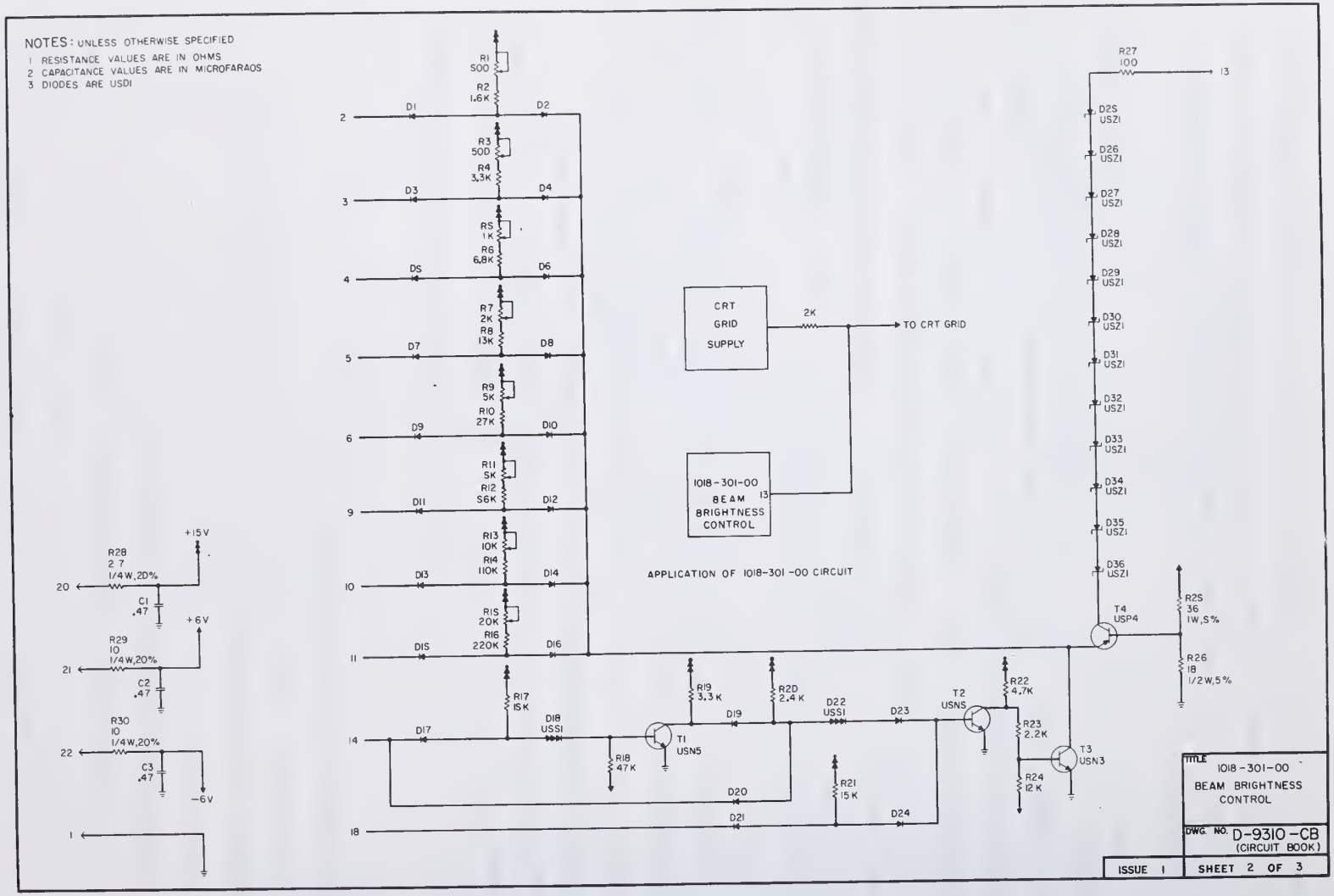
NOTES: UNLESS OTHERWISE SPECIFIED
1 RESISTANCE VALUES ARE IN OHMS
2 CAPACITANCE VALUES ARE IN MICROFARADS
3 DIODES ARE USDI
R1 500
R2 1.6K
R3 50D
R4 3.3K
R5 1K
R6 6.8K
R7 2K
R8 13K
R9 5K
R10 27K
R11 5K
R12 56K
R13 10K
R14 110K
R15 20K
R16 220K
R17 15K
R18 47K
R19 3.3K
R20 2.4K
R21 15K
R22 4.7K
R23 2.2K
R24 12K
R25 36 1W,5%
R26 18 1/2W,5%
R27 100
R28 2.7 1/4W,20%
R29 10 1/4W,20%
R30 10 1/4W,20%
C1 .47
C2 .47
C3 .47
D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23 D24
D25 USZI
D26 USZI
D27 USZI
D28 USZI
D29 USZI
D30 USZI
D31 USZI
D32 USZI
D33 USZI
D34 USZI
D35 USZI
D36 USZI
T1 USN5
T2 USN5
T3 USN3
T4 USP4
+15V
+6V
-6V
CRT GRID SUPPLY
2K
TO CRT GRID
1018-301-00 BEAM BRIGHTNESS CONTROL
13
APPLICATION OF 1018-301-00 CIRCUIT
TITLE
1018-301-00
BEAM BRIGHTNESS CONTROL
DWG. NO. D-9310-CB
(CIRCUIT BOOK)
ISSUE 1
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FIGURE 31

(and it is a pulse) that ultimately results from a single electron leaving the cathode can vary greatly in magnitude since the "multiplier" is actually twelve cascaded multipliers, each having a statistical distribution of integer gains. Thus, on this time scale the PMT output will appear very noisy. (By way of contrast, the astronomer can integrate over a period of minutes and thus use very high gains effectively.)

The subject of quantum noise in PMT's is a complex one treated at length in various journals. Unfortunately, most analyses deal with detection of single events of low level (scintillators) or other applications too remote from CRT flying spot scanners to be immediately applicable. In any case, useable signal to noise ratios in this application necessitate PMT supply voltages not higher than 1500 volts.

The manufacturer's rated maximum anode current for the RCA 8575 PMT is 200 μA averaged over a 30 second interval. As a matter of good engineering practice, anode current should be limited to one half the rated value to provide some latitude for measurement error, drift in operating points and transients. Restricting anode current to one half the rated value does not guarantee safe and satisfactory operation, however. RCA data indicate that similar tubes operated at 100 μA anode current show diminished sensitivity (short-time fatigue) of about 30% in 100 minutes of operation. A recovery period of several hours will restore most of the loss. Operation for 500 hours at this level will reduce sensitivity permanently by about 70%. The RCA data sheet for the 8575 suggests that best stability will be obtained with anode currents less than .1 μA. For a 2000 volt supply voltage this would be .15 electron/μsec.

Power for the PMT is provided by the circuit shown in Figure 32, a simple but satisfactory voltage divider. More complicated configurations using zener diodes or an adjustment for the focusing electrode potential do not appear to add significantly to performance.

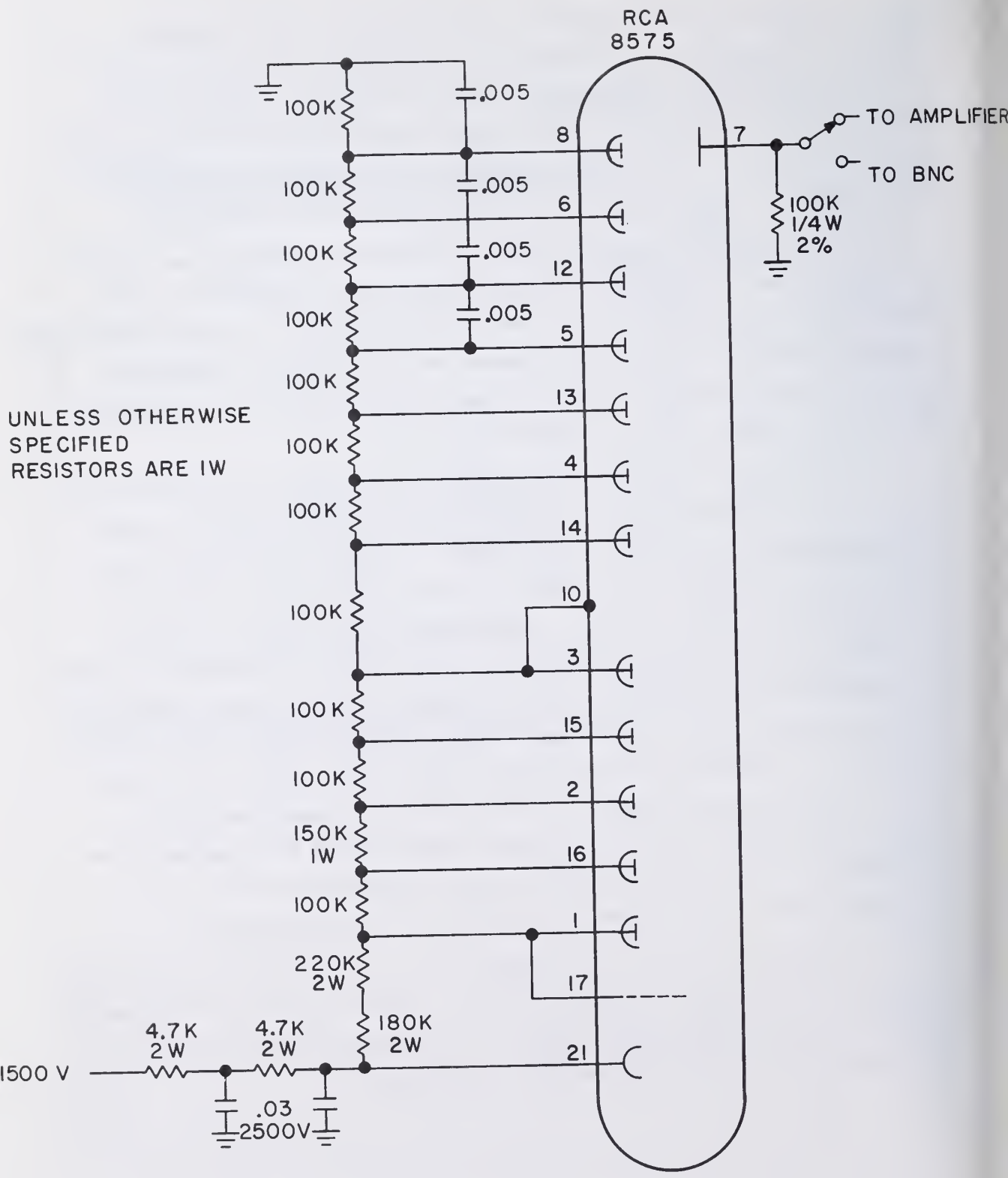

RCA
8575
100K
.005
8
7
TO AMPLIFIER
TO BNC
100K
1/4W
2%
100K
.005
6
100K
.005
12
100K
.005
5
100K
13
UNLESS OTHERWISE
SPECIFIED
RESISTORS ARE 1W
100K
4
100K
14
100K
10
3
100K
15
100K
2
150K
1W
16
100K
1
220K
2W
17
4.7K
2W
4.7K
2W
180K
2W
1500 V
21
.03
2500V

FIGURE 32

The photomultiplier amplifier (box 25) is shown in Figure 33. Essentially, it is an inexpensive IC op amp connected as a transresistance of 40K. That is, the output voltage is the product of the PMT anode current and the feedback resistance, 40K. The emitter follower output transistor is capable of driving a terminated 95 ohm coax line.

A few remarks about the nonobvious features of Figure 33 are appropriate. The 100K pot is needed to cancel the variable offset current of the μ702. The test BNC allows the amplifier to be tested realistically; the 47 ohm resistor serves as termination for a pulse generator, the 100K makes the pulse generator appear to be a current source. The DC OUT BNC terminal provides a voltage proportional to the average PMT anode current. The RC filtering merely minimizes the flicker in the DVM used to monitor this quantity.

The desirability of mounting the PMT amplifier physically close to the PMT follows more or less naturally from the nature of the PMT signal. The anode current is small and the source impedance is high, conditions which militate against sending this signal over long distances. Less obvious are the factors governing the placement of other signal conditioning elements. Why not place all of them (boxes 24 through 29) in a single assembly near the PMT? To see some of the problems inherent in this approach consider the highly simplified configuration of Figure 34.

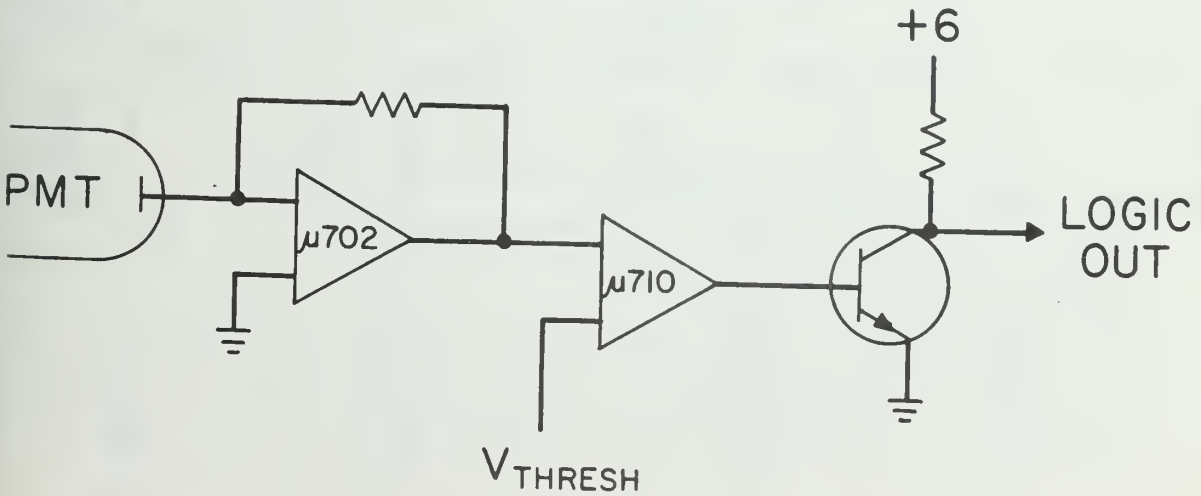
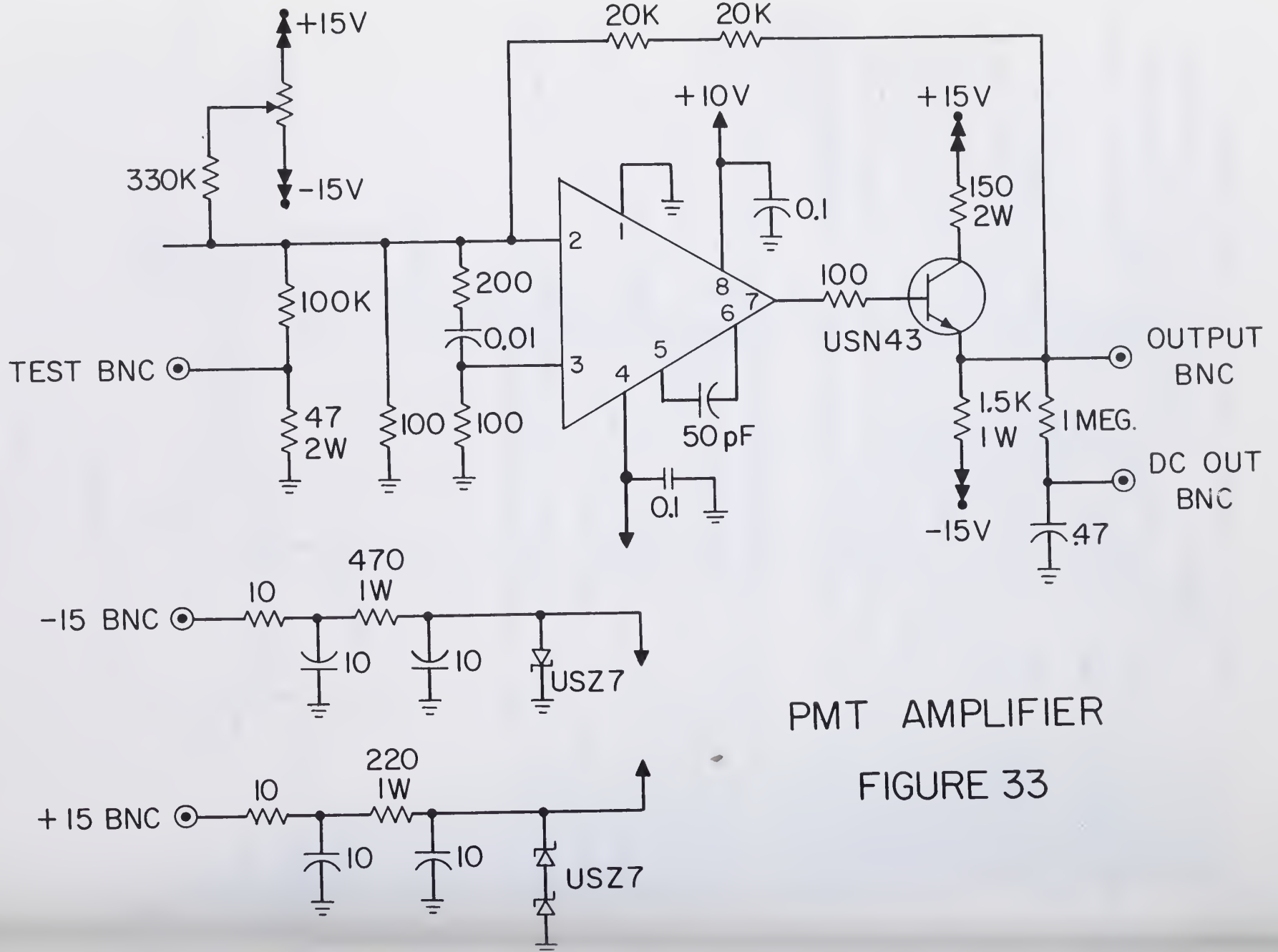


FIGURE 34



PMT AMPLIFIER

FIGURE 33

Here we have an amplifier (transresistance) followed by a voltage comparator. For PMT currents greater than some threshold, the logic output will be at its most positive value. The difficulty arises with PMT currents which just reach the threshold value. Under this condition, the comparator has a voltage gain of about 2000 and the current gain of the complex (measured from PMT anode to collector of the output transistor) can easily exceed 10^7. If there exists the slightest unintended coupling between input and output (through common grounds, common power supplies, etc.) the system will oscillate for some input current range.

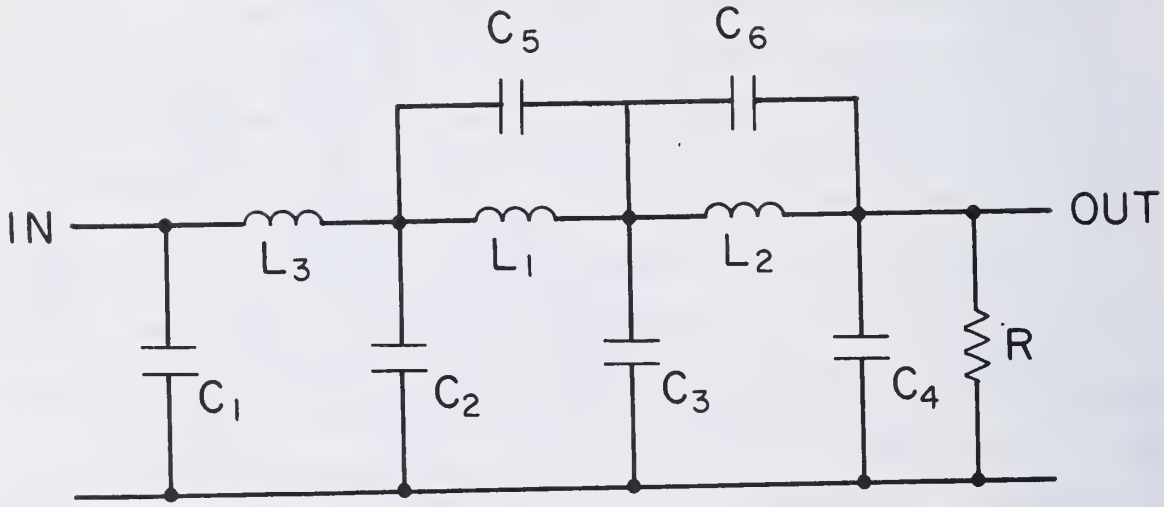
It is certainly possible to package the system of Figure 34 in one housing by carefully decoupling the circuits. In a practical case, however, it is much simpler to physically separate the parts. Physical separation brings other benefits such as easier accessibility.

The output of the PMT amplifier can be regarded as useful signal combined with noise due to the granularity of the CRT phosphor and quantum noise from the PMT. The multi-section LC filter shown in Figure 35 takes advantage of the different spectra of these components to improve the signal to noise ratio. Filters of this type are called $\sin^2$ filters from their property of converting an input impulse function into a bell shaped $\sin^2$ output.

A $\sin^2$ filter is defined by its impedance and a characteristic period, T. In simplest terms, any rectangular pulse of greater duration than T is transmitted with little attenuation. Pulses of width t narrower than T are attenuated by approximately t/T.

Obviously, the spectrum of the useful signal depends both on the nature of the scanned image and on the scanning speed. It is thus necessary to provide a family of $\sin^2$ filters for various applications.

The light output of a CRT is likely to be nonuniform from point to point on the screen owing to initial phosphor irregularities as well as the burn and wear out deteriorations mentioned earlier. In addition,


C5
C6
IN
OUT
L3
L1
L2
R
C1
C2
C3
C4

there may be nonuniformities in the optical system connecting the CRT and PMT (e.g., vignetting). This being true, there must be some means of distinguishing between PMT signals due to image opacity and PMT signals due to CRT light output variations.

One method of cancelling the effect of CRT variation is indicated in Figure 1. Two identical PMT's are provided, one receiving light through the image and one receiving light through a similar optical path but not through the image. A signal equal to the ratio of the outputs of the two PMT's is then a true measure of the opacity of the image.

Division of two analog voltages can be accomplished in various ways such as that shown in Figure 36.

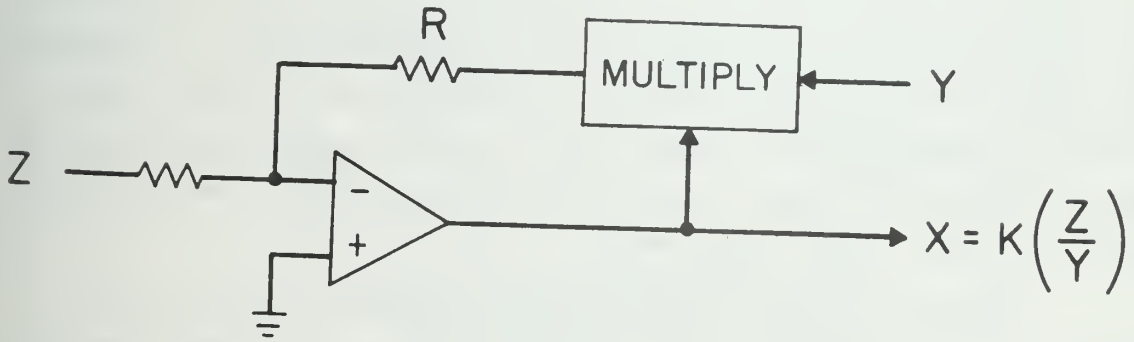


FIGURE 36

This approach has the disadvantage that it is not symmetric for the two inputs. That is, the delays associated with Y and Z are likely to be unequal with the result that for fast transients the output may be inaccurate.

The configuration partially shown in Figure 1 forms the ratio as the antilog of the difference of the logarithms of the inputs. This approach allows the use of identical amplifiers and filters for the two PMT's. Thus, if a "hot grain" (a small area of the phosphor with high light output) causes a momentary increase in light output, the resulting PMT signals will reach the subtraction and antilog circuits (box 28) together. This makes it possible to cancel the effect of variable light output over a fairly wide range.

The logarithmic amplifier shown in Figure 37 is based on the logarithmic relation between collector current and base-emitter voltage. For two matched transistors operating at different collector currents

$$\Delta V_{BE} = \frac{kT}{q} \ln \left(\frac{I_{c1}}{I_{c2}}\right)$$

In the circuit of Figure 37, I_{c1} is made proportional to the input voltage, I_{c2} is a constant and ΔV_{BE} is amplified to provide the output. Temperature coefficient of the circuit is necessarily high since ΔV is proportional to the absolute temperature, T. This is not a serious problem since both log amps are mounted on a single printed circuit card and are therefore subjected to the same ambient temperature.

The subtraction and exponentiation functions of box 28 can be realized with the circuit shown in Figure 38. The first op amp forms the difference of the inputs; the second op amp uses the logarithmic property of D1 to provide an output of the form K exp (V_1-V_2). Diode D2 is used only for thermal compensation.

There are many clever and interesting techniques for converting an analog voltage to a digital representation. It is fairly easy to show, however, that where the number of bits encoded is small, the best approach is the "brute force" method of 2^N parallel voltage comparators. This method is particularly attractive now that IC comparators are quite inexpensive

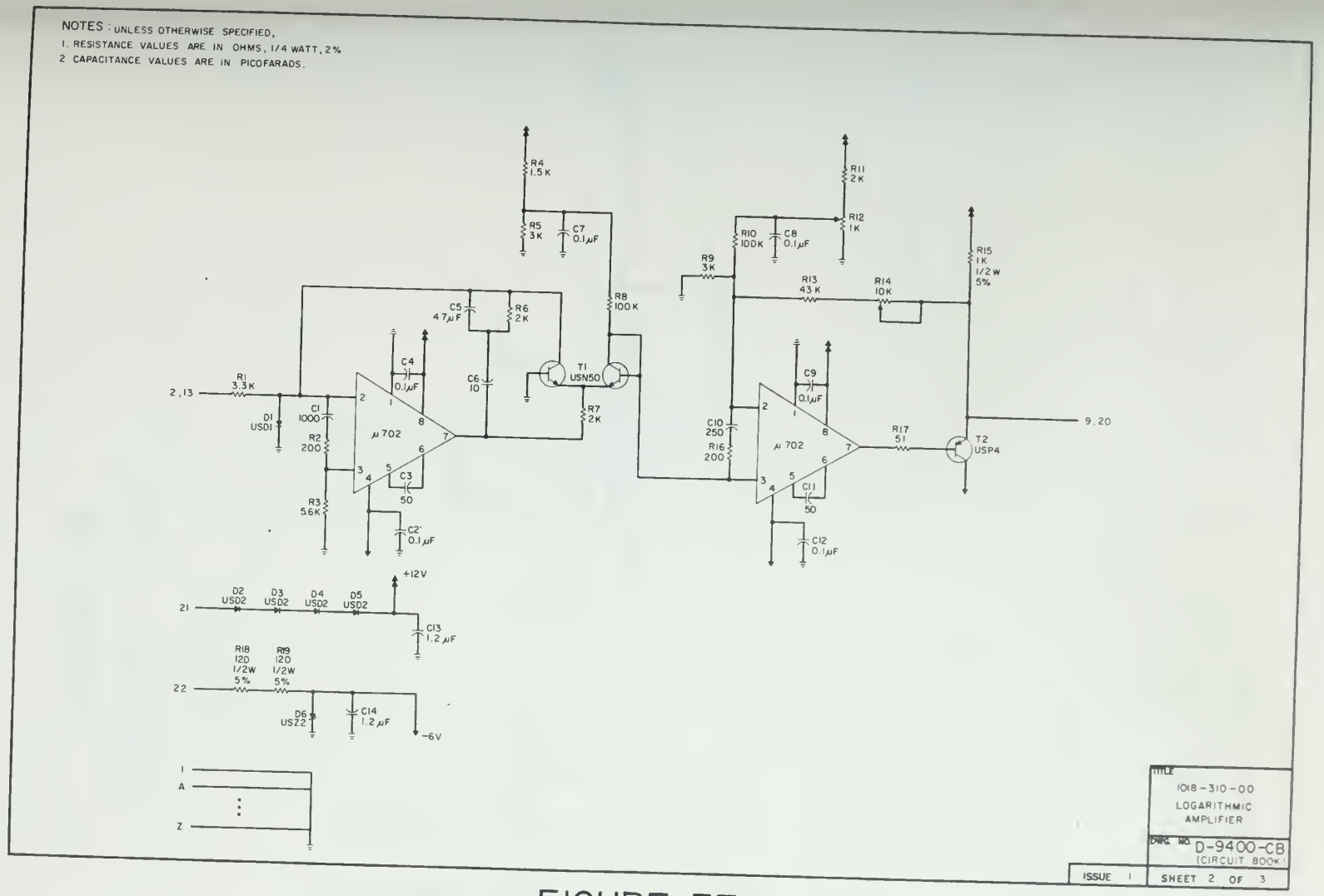
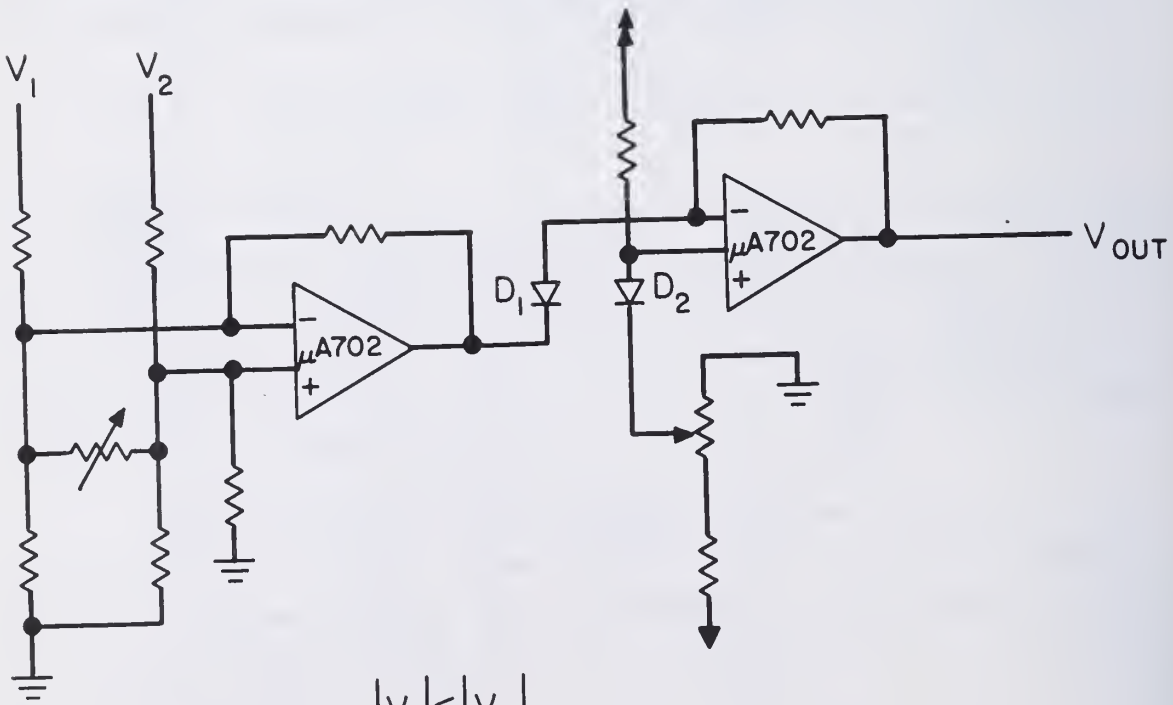

NOTES : UNLESS OTHERWISE SPECIFIED,
1. RESISTANCE VALUES ARE IN OHMS, 1/4 WATT, 2%
2 CAPACITANCE VALUES ARE IN PICOFARADS.
R4 1.5K
R5 3K
C7 0.1µF
R11 2K
R12 1K
R10 100K
C8 0.1µF
R9 3K
R13 43K
R14 10K
R15 1K 1/2W 5%
C5 47µF
R6 2K
R8 100K
C4 0.1µF
C6 10
T1 USN50
C9 0.1µF
2,13
R1 3.3K
C1 1000
D1 USD1
R2 200
µ 702
C3 50
R3 5.6K
C2' 0.1µF
R7 2K
C10 250
R16 200
µ 702
R17 51
T2 USP4
9,20
C11 50
C12 0.1µF
+12V
21
D2 USD2
D3 USD2
D4 USD2
D5 USD2
C13 1.2µF
R18 120 1/2W 5%
R19 120 1/2W 5%
22
D6 USZ2
C14 1.2µF
-6V
I
A
Z
TITLE
1018-310-00
LOGARITHMIC
AMPLIFIER
DWG NO D-9400-CB
(CIRCUIT 800K)
ISSUE 1
SHEET 2 OF 3

FIGURE 37



ANTILOG CIRCUIT

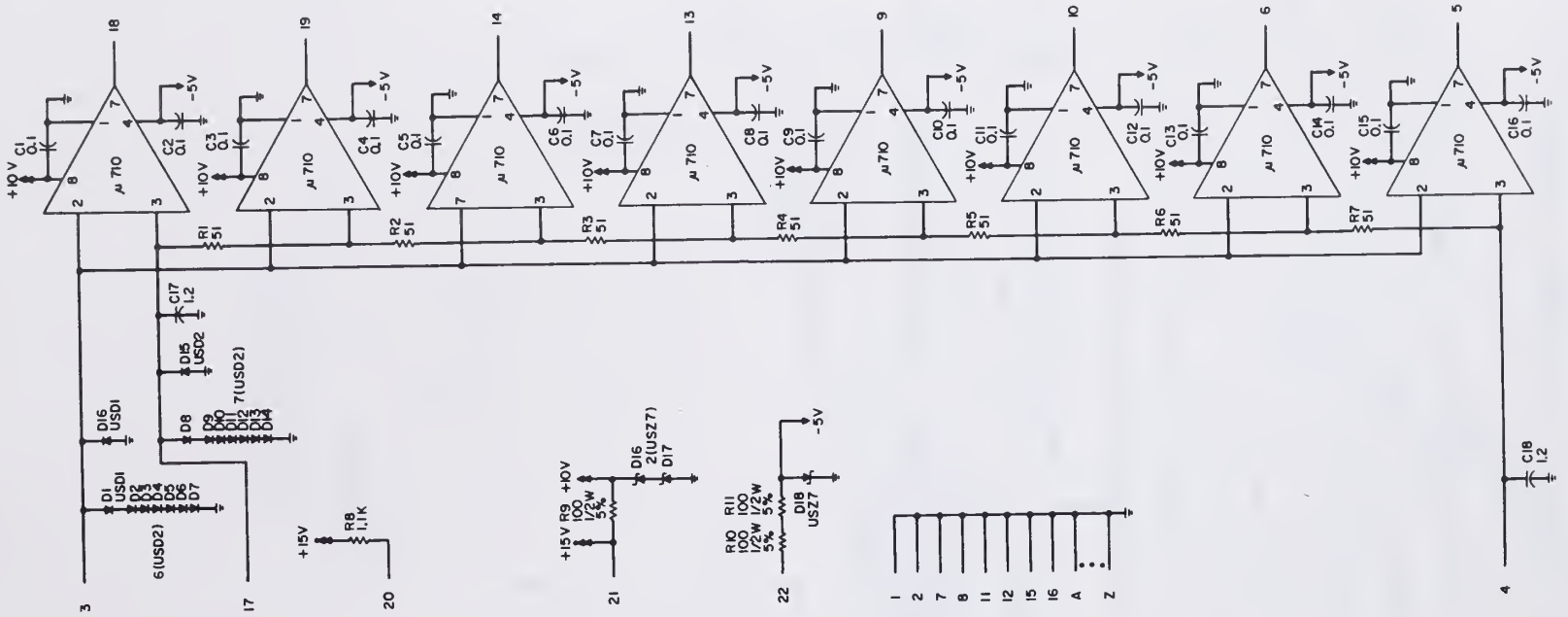
FIGURE 38

For the present, the Illiac III scanners provide only four bits of gray scale information. The necessary sixteen comparators (actually, only fifteen are necessary) are handily packaged on two printed circuit cards of the type shown in Figure 39.

Box 29 consists of the aforementioned comparator cards, cards for amplifying the μ710 outputs up to logic level voltages, inverters and diode matrix cards for converting the unary output of the 313 cards into the customary binary notation. The complex totals eight printed circuit cards including the high current line driver card. While this is not an extremely compact realization, one very important feature should be noted. All of the circuits in box 29 are combinatorial, the type of logic most easily checked out and maintained.

A fringe benefit of this organization follows from the method of setting threshold voltages for the comparators. The voltages in the reference voltage chain (obtained from the string of 51 ohm resistors) could be separately specified to provide a nonlinear conversion, perhaps with program-controlled nonlinearity.

NOTES: UNLESS OTHERWISE SPECIFIED —
1. RESISTANCE VALUES ARE IN OHMS, 1/4 WATT, 2%.
2. CAPACITANCE VALUES ARE IN MICROFARADS



TITLE	1018-313-00 ADC 'FOR PMT
DWG. NO.	D-9430-CB (CIRCUIT BOOK)
ISSUE 1	SHEET 2 OF 3

FIGURE 39

APPENDIX I

Adjustment of DAC Cards

The test fixture for 1018-300-00 and 1018-306-00 cards incorporates test circuits for DC adjustments and for timing adjustments. Aside from power supply connections these two circuits are completely independent. The circuits are shown in Figures I.1 and I.2.

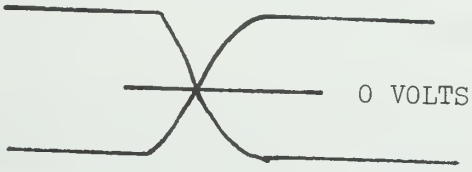
In making the initial tests and groupings, the total set of cards will be measured and adjusted at one time. This will permit sorting the 300 cards into well-matched sets of three.

1) Place a 300 card in the timing adjustment socket of the test fixture.

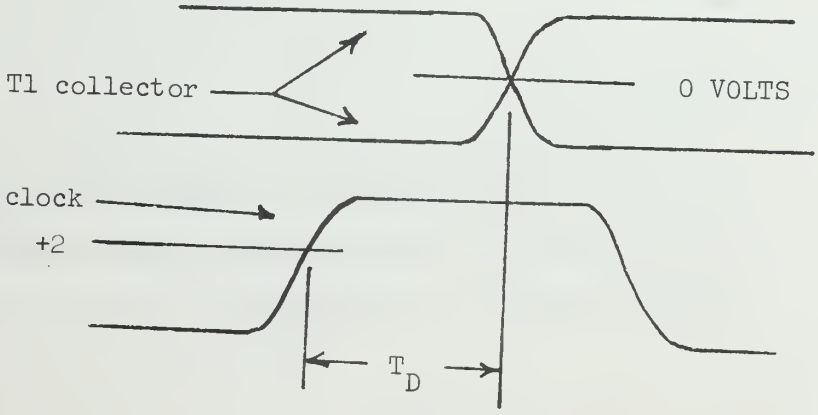
2) Set Datapulse 101 to approximately 1 mc., 50% duty cycle, 6 volt position pulse.

3) Sync Tektronix 454 on output of 308 clock driver.

4) Look at collector of T1 on 300 card, adjust R12 for rise and fall intersection at zero volts. It may be necessary to readjust Datapulse frequency to insure that both transitions are seen.



5) Measure and record stage delay in nanoseconds



6) Repeat for collectors T3, T5 and T7 while adjusting R15, R18 and R21.

7) Complete timing adjustments for all cards before commencing DC adjustments.

8) Document each set selection including which is most significant, which is least. On the basis of T_D, group the cards into sets of three. (The most uniform sets will be used in the scanners; the others will be used in monitors.)

9) Place the most significant 300 from any set in the most significant DC adjustment position of the test fixture. Insert 306 op amp card.

10) Apply power to test fixture and to Dana 5500 DVM for a minimum of one hour before making measurements.

11) S1 on 306 should be closed.

12) On test fixture, switches 0 through ID down, sw 11 up, adjust R12 on 306 for zero voltage on pin 6 of 306. This should be adjusted carefully to a few μV.

13) Open S1 on 306.

14) Set Khron-Hite supply for exactly 36.000 volts.

15) Data switches still set to 1000 0000 0000.

16) Adjust R24 on 300 card for 4.0960 volts on pin 12 of 306 card. This should be near the center of the adjustment range of R24.

17) Set data switches to 0000 0000 0000. Output should be less than one mv. If output is not exactly zero, return to step 16 and adjust R24 for an output voltage 4.0960 volts more positive than the nominal zero.

18) Set data switches to 0100 0000 0000.

19) Adjust R27 for 2.0480 volts (relative to nominal zero).

20) Set data switches to 0010 0000 0000.

21) Adjust R31 for 1.0240 volts (relative to nominal zero).

22) Set data switches to 0001 0000 0000.

23) Adjust R35 for .5120 volts (relative to nominal zero).

24) Remove power just long enough to move this 300 card to the middle significance DC adjustment position. If the power is not off longer than ten seconds, allow one minute before continuing adjustments.

25) Set data switches to 0000 1111 0000.

26) Adjust R9 of the 306 card for an output of 480.0 mv relative to nominal zero.

27) Remove power briefly, move the 300 card to the least significant DC adjustment position.

28) Set data switches to 0000 0000 1111.

29) Adjust R13 of 306 card for output of 30.0 mv relative to nominal zero.

30) Move 300 card back to most significant DC test slot and recheck outputs of 4.0960, 2.0480, 1.0240 and .5120 volts.

31) Set this 300 card aside.

32) Place the middle significance 300 card from the same set into the most significant DC adjustment slot.

33) Set data switches to 1000 0000 0000.

34) Repeat steps 16 through 23.

35) Set this 300 card aside.

36) Place the remaining 300 card of this set into the most significant DC adjustment slot.

37) Set data switches to 1000 0000 0000.

38) Repeat steps 16 through 23.

39) Place the three 300 cards in the DC adjustment positions in the correct order.

40) Check the output for the following input values.

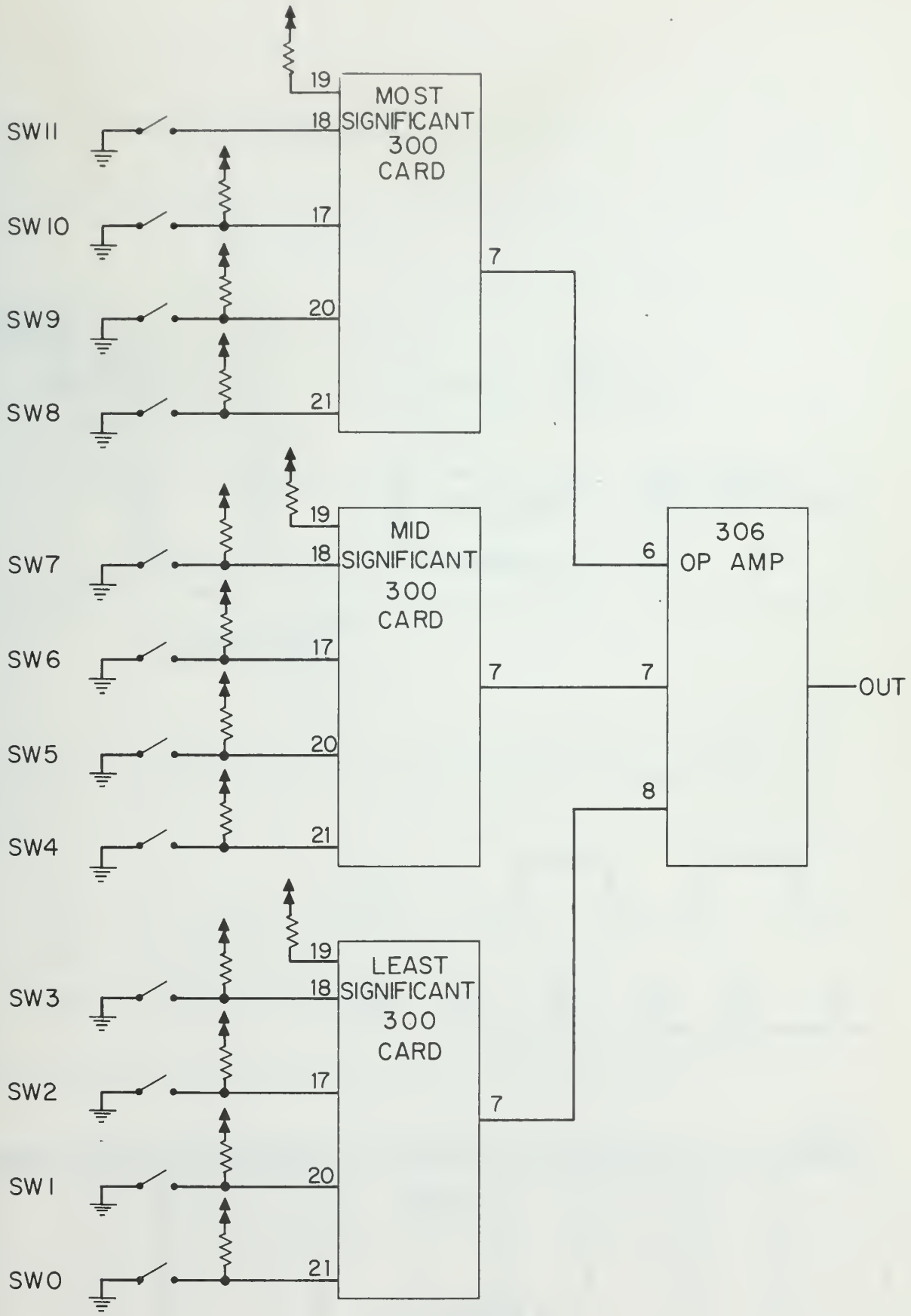
Switches	Output
0000 0000 0000	0.0000
1000 0000 0000	4.0960
0111 1111 1111	4.0940
0100 0000 0000	2.0480
0011 1111 1111	2.0460
1100 0000 0000	6.1440
1011 1111 1111	6.1420

41) Close S1 on the 306 card.

42) Set data switches to 1111 1111 1111.

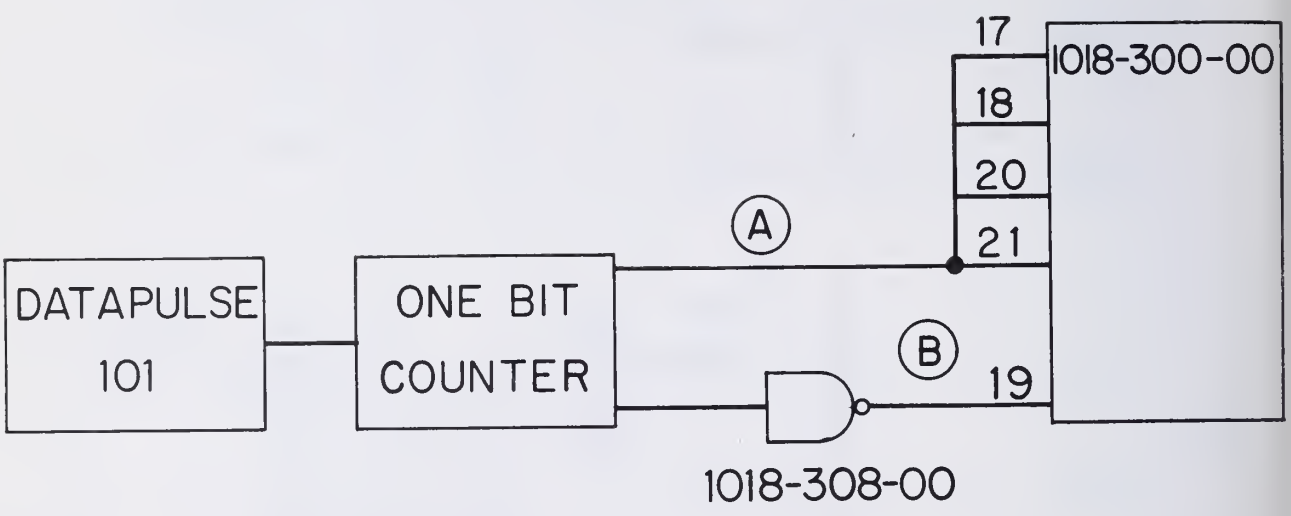
43) Adjust R5 on the 306 for an output of zero.

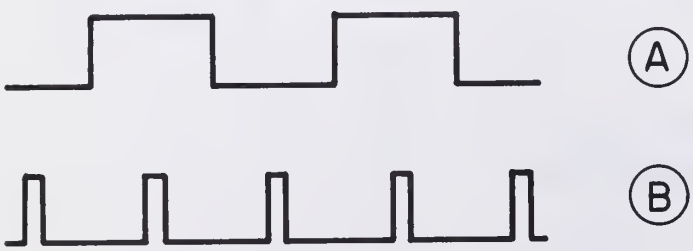
44) The three 300 cards and the 306 card make up one set. Record by serial numbers.



DC ADJUSTMENT FIXTURE FOR 1018-300-00 CIRCUIT CARD.

FIGURE I.1





TIMING ADJUSTMENT FIXTURE FOR 1018-300-00 CIRCUIT CARD

FIGURE I.2

APPENDIX II

Testing and Sorting of TD 101's for Use in the
1018-300-00 Card

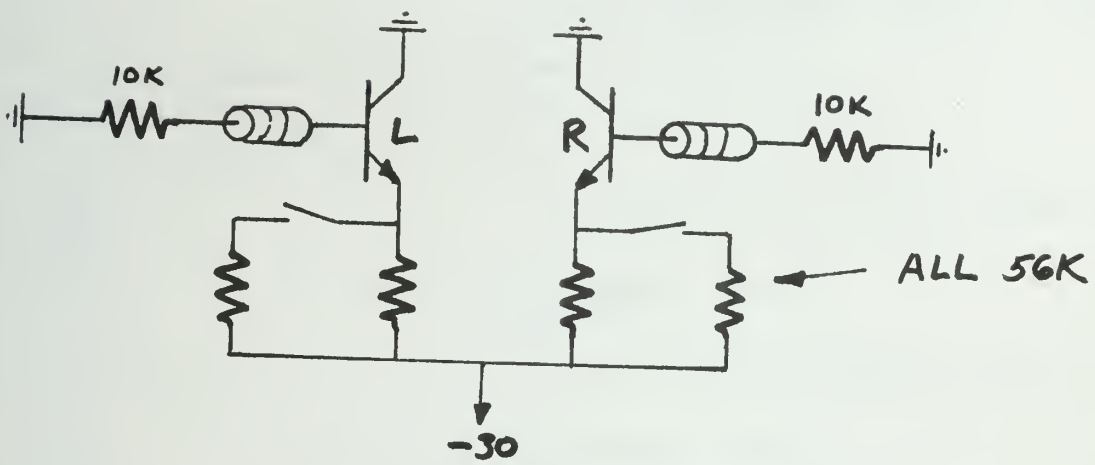


FIGURE II.1

Using the test facility shown above, measure base and emitter voltages for two values of emitter current, a total of eight measurements for each TD 101.

VBL - Base voltage, left side
VBR - Base voltage, right side
VEL - Emitter voltage, left side
VER - Emitter voltage, right side

Tabulate measured and calculated values in the following order

	#	VEL	VBL	VBEL		VER	VBR	VBER		VBEL -VBER
.5MA										
1MA										
.5MA										
1MA										

VBEL = VEL-VBL

VBER = VER-VBR

Select a transistor Ⓔ such that

|VBEL-VBER|<3 mv at 1 ma

VBL <40 mv at 1 ma

VBR <40 mv at 1 ma

Now, choose a transistor Ⓕ such that

|VBLⒺ - VBRⒻ|< 1mv at 1 ma

Then, choose a transistor Ⓖ such that

|VBL Ⓖ - VBL Ⓕ |<2 mv at .5 ma

and |VBEL Ⓖ - VBER Ⓖ |<3 mv at .5 ma

This makes up one set which must be documented and preserved as a set for installation in a 1018-300-00 card. After the requisite number of such sets have been chosen, the remaining TD 101's are sifted for the Ⓐ, Ⓑ, Ⓒ and Ⓓ positions. Transistors for Ⓐ and Ⓒ meet the specifications

VBL<25 mv at .5 mv

VBR<25 mv at .5 ma

|VBEL - VBER |<3 mv at .5 ma

and transistors for Ⓑ to Ⓓ meet

VBL<50 mv at 1 ma

VBR<50 mv at 1 ma

|VBEL - VBER |<3 mv at 1 ma

Document selections and assemble into sets of seven.

APPENDIX III

Testing and Grouping DTS-410 Transistors

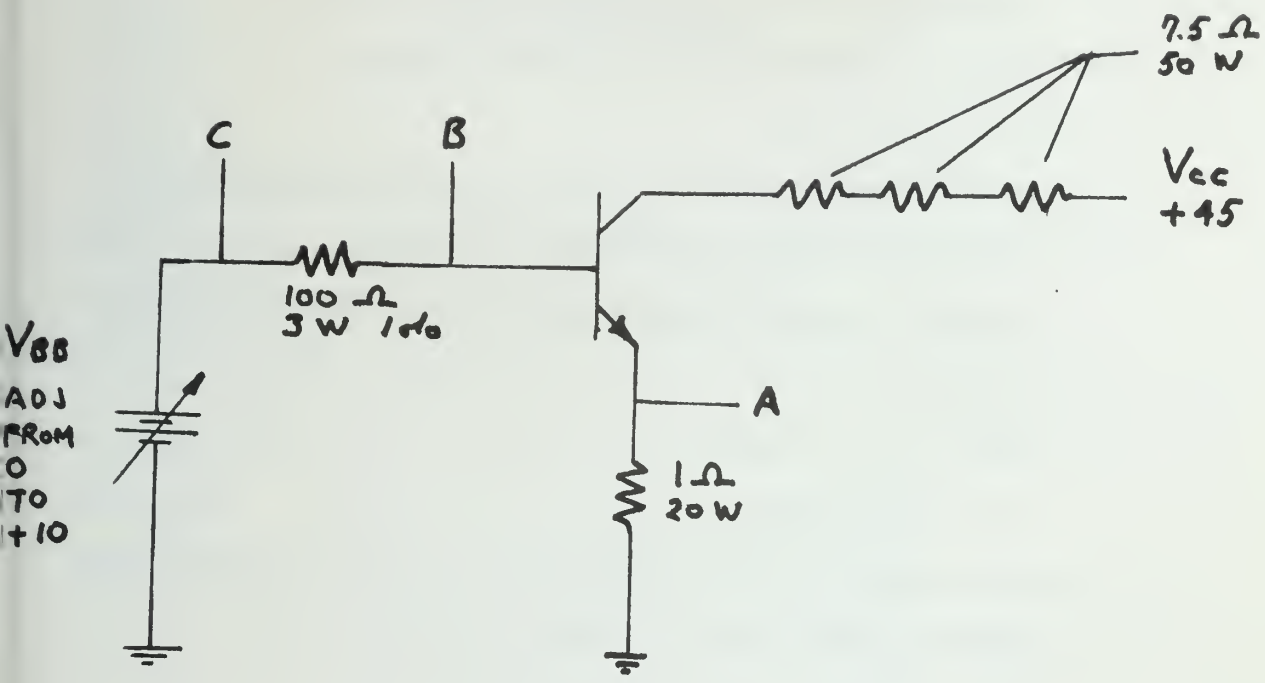


FIGURE III.1

All of the DTS-410's used in the deflection amplifiers were tested using the circuit shown above. The fixture includes a clamp to securely hold the transistor against the air-cooled heatsink.

1) Clamp DTS-410 to heatsink.

2) Apply V_{CC}.

3) Increase V_{BB} from zero until V_A = 1.000 volts

4) After one minute, with V_A still equal to 1.000 volt, read V_B and V_C and record.

5) Recheck V_A.

6) After all transistors are measured, calculate $V_C - V_B$ for each.

7. On a very large sheet of graph paper plot each transistor as a point. Abscissa represents base-emitter drop (V_B-1.000). Ordinate represents base current, which is proportional to $V_C - V_B$.

8) Draw a line of negative slope based on 100 mv vertically for 30 mv horizontally.

9) Group transistors into triplets on the basis of "closeness". Closeness can be defined using Figure III.2

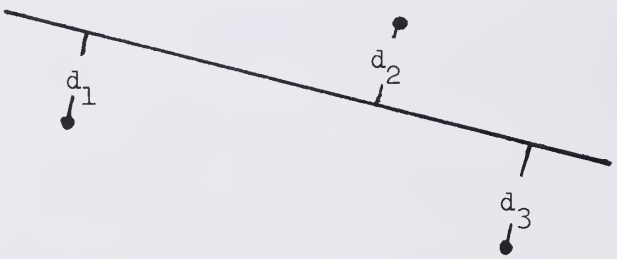


Figure III.2

For a set of three points, draw a line parallel to the line of step 8 which minimizes $d_1^2 + d_2^2 + d_3^2$. The function $d_1^2 + d_2^2 + d_3^2$ is a measure of closeness of matching. (The extent to which two points are close to the same line merely indicates the extent to which their differences in V_{BE} are compensated by the drops in their respective base resistors. Note that the slope is based on the 30 ohm base resistor of the amplifier, not the 100 ohm resistor of the test fixture.)

APPENDIX IV
INPUT, OUTPUT AND OTHER SPECIFICATIONS
FOR ANALOG BOXES

Box 1, X and Y Registers

Input: Logic signals for incrementing, decrementing, scale change.

Output: Logic level (0 to +6), single sided.

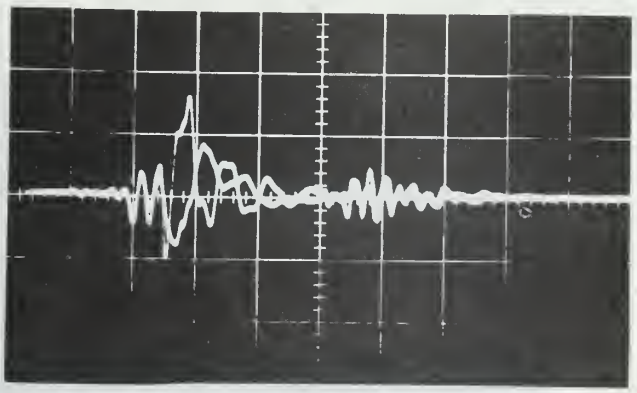
Notes: Register is part of a double-rank, bi-directional counter with facilities for counting by units, twos, fours, etc.

Box 2, DAC

Input: Logic level signals for data, clock. Data signals must be current limited for positive going signals. Requires special power supply voltages of +15, -15, -3, -39 in addition to normal logic supply voltages.

Output: Analog voltage in the range 0 to -8.190 volts from low impedance source.

Settling Time: Worst case settling time (for transition from 2047 to 2048) shown in photo below.



Tempco: Temperature coefficient of entire DAC (excluding power supplies) measured to be 5 PPM/^{o}C in the range 27^{o}C to 37^{o}C.

Notes: When boxes 1 and 2 are physically remote it will be necessary to drive the connecting cable with 214-02 drivers since line capacitance would slow a DTL driver excessively. This will in turn necessitate a DTL buffer at the box 2 end since inputs to box 2 must be current limited. Photo below shows output of unloaded SN 7475N with the transition directions superimposed.

1 V/DIV

10 NS/DIV

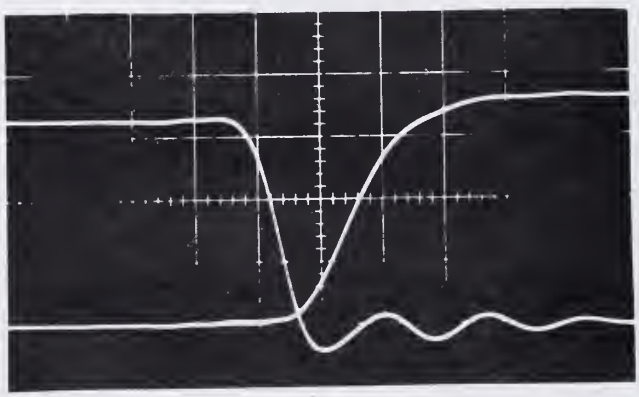
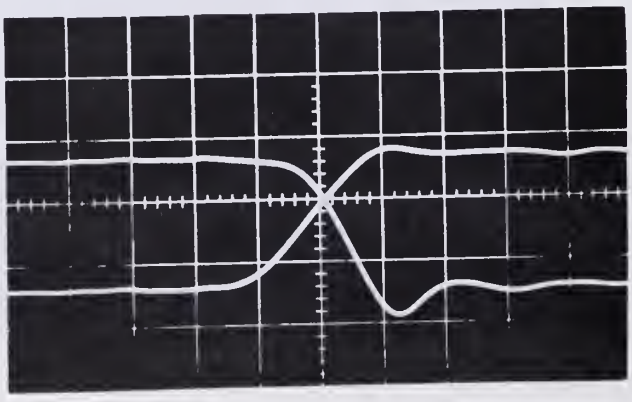


Photo below shows collector of T1 when R12 adjusted for transition crossing at 0 volts.

1 V/DIV

10 NS/DIV



Box 3, Preamp

Input: Two analog signals (gross and vernier), each 0 to -8.190 volts.

Output: Pushpull analog signals. Exact specification not pertinent since this is inside a feedback loop.

Box 4, Deflection Amplifier

Input: Analog signals from preamp.

Output: Pushpull analog currents adjustable up to a twelve ampere swing (i.e. from 0, +6 to +6, 0).

Box 5, Deflection Yoke

Input: Current from deflection amplifier.

Output: Magnetic field.

Notes: Celco HDS 428-P670-1
half axis values
R = .15 ohm
L = 25 μH
C = 60 pF

Box 6, Theta Register

Input: Logic signals for incrementing, scale change.

Output: Eight logic-level signals, double sided. Interpret as integers from 0 to 255, with the least significant five bits called N.

Box 7, Complement Gate

Input: Logic signals including dummy inputs.

Output: Eight logic-level signals, single sided.

Box 8, Ladder Drivers

Input: Logic signals from box 7.

Output: Eight lines, each of which is at zero volts or -15 volts.

Box 9, Ladder

Input: Switched voltages from box 8.

Output: Analog voltage from zero to (255/256)(-15 volts) with 1K source impedance. For even numbered octants V = N/32 (-15) volts. For odd numbered octants V = (31.875-N)/32(-15) volts.

Box 10, SINE Generator

Input: Analog voltage from box 9.

Output: For even numbered octants $V = 10.607\sin\left(\frac{N}{32} \quad \frac{\pi}{4}\right)$volts.

For odd numbered octants $V = 10.607\sin\left(\frac{31.875-N}{32} \quad \frac{\pi}{4}\right)$volts.

Both positive and negative outputs are available from low impedance sources.

Box 11, COSINE Generator

Input: Analog voltage from box 9.

Output: Remarks of box 10 apply if sin is replaced by cos.

Box 12, Function Selector

Input: Three logic-level signals, four analog signals.

Output: Two analog signals identical in value to two of the analog input voltages.

Notes: This box includes part of a 214-02 card and a 236-24 diode matrix card in order to decode the octant information.

Box 13, Attenuator

Input: Analog voltage in the range +10.607 to -10.607 volts, eight logic-level signals. Logic signals to be interpreted as an integer, K, between 0 and 255. (Values of K larger than 128 will not be used.)

Output: Analog voltage in the range +1.5 to -1.5 volts

$$V_{OUT} = V_{IN} \frac{K}{256} .283$$

Notes: Each of the eight logic signal input is actually a triple diode "and" to facilitate encoding.

Box 14, Theta Amplifier

Input: Analog voltage from box 13, special power supply voltages of +20 and -20.

Output: Single ended current in range +1.5 amp to -1.5 amp.

Notes: Celco DA-PP2B

Box 15, Diquadrupole Coil

Input: Current from box 14.

Output: Magnetic field.

Notes: Celco B-1700-8
half axis value
R = .43 ohm
L = 160 μH

Box 16, Dynamic Focus Correction

Input: Analog voltages from gross X and Y DAC's.

Output: Analog voltage proportional to $(X^2 + Y^2)$ where X and Y are deflections relative to center screen.

Box 17, Focus Amplifier

Input: Analog voltage from box 16, box 20, power supply voltages of +20 and -20.

Output: Single ended analog current.

Notes: Celco DA-PP2B

Box 18, Focus Coil

Input: Current from constant current supply, analog signal from box 17.

Output: Focusing field

Notes: Celco B-1613-2
static focus
R = 5.2 ohm
L = 25 mH.
dynamic focus
R = 2.1 ohm
L = 294 μH

This is a special irrotational design necessitated by the diquadrupole coil.

Box 19, Line Width Register

Input: Logic-level signals.

Output: Two bits, double sided logic-level.

Box 20, Defocus

Input: Logic signals from box 19.

Output: One of four analog current values. One of the values must be zero, the other three can be of the form

$$I_{OUT} = D_N I_D$$

where D_1, D_2, D_3 are integers in the range 0 to 255, I_D is a constant.

Note: For circuit simplicity, all defocus currents are offset by a fixed amount. The "zero" defocus state actually represents the greatest output current from the 301-01 card.

Box 21, Brightness Register

Input: Logic-level signals.

Output: Eight logic-level lines, single sided.

Box 22, Beam Brightness

Input: Eight brightness signals from control logic, eight brightness signals from toggle switches, 3 control lines from toggle switches, one logic signal for phosphor protection.

Output: An analog current which, when used with a suitable power supply and an external resistor, will modulate the CRT grid voltage over a range of 25.5 volts in .1 volt steps.

Notes: This box includes the beam brightness card, 301-00, other logic cards and switches for manually adjusting the operating point.

Box 23, CRT

Input: Grid -- approximately -100 volts
First anode -- 2KV
Second anode -- 20 KV

Output: Blue to UV light

Notes: Litton Industries L4123.

Box 24, Photomultiplier

Input: Typical supply voltage = 1500 volts.

Output: Maximum of 100 μA.

Notes: RCA 8575

Box 25, PMT Amplifier

Input: Current from PMT

Output: Voltage in range 0 to +4 volts.

Notes: Amplifier is essentially a transresistance of 40K.

Box 26, Filtering

Input: From box 25

Output: Attenuated and smoothed version of input

Notes: Any of several filters can be used here. All are of $\sin^2$ type.

Box 27, Logarithmic Amplifier

Input: Analog voltage in range +.02 to +2 volts.

Output: Analog voltage in range 0 to +2 volts.

$$V_{OUT} = \log \frac{V_{IN}}{.02}$$

Box 28, Antilog

Input: Analog signals from logarithmic amplifiers in the signal PMT chain and the reference PMT chain.

Output: Analog voltage proportional to the ratio of signal PMT output to reference PMT output.

$$V_{OUT} = [10^{(V_R - V_S)}]_H$$

where V_R and V_S are the reference and signal outputs of their respective log amps. H to be experimentally established.

Box 29, Analog to Digital Conversion

Input: Analog voltage in range 0 to +4 volts.

Output: Four bits of gray scale information.

APPENDIX V

Semiconductors Used in Illiac III Circuits

All of the semiconductors appearing on Illiac III circuit drawings are described by a unified designator system as follows:

U -- Universal description system
G,S -- Germanium or Silicon
N,P,D,S,Z -- NPN transistor, PNP transistor, diode, stabistor (multi-junction diode), zener diode.

The final numerals are assigned in sequence, by class, as semiconductors are added to our semiconductor directory.

For the benefit of readers outside the Department, the semiconductors appearing in this note are listed with their approximate JETEC equivalents or other description. In many cases, the U designated device is selected from the 2N device listed.

USN3 - 2N2369
USN4 - 2N2219
USN48 - 2N3704
USN49 - SPRAGUE TD101
USP4 - 2N3702
USP15 - 2N4423
UGN4 - 2N1308
UGP1 - 2N964
UGP15 - 2N1309
USD1 - HIGH SPEED SILICON LOGIC DIODE
USD2 - SLOW SILICON DIODE, LEVEL SHIFTER
USS1 - THREE SLOW SILICON DIODE JUNCTIONS IN ONE PACKAGE
USZ5 - IN749 (4.3v)
USZ6 - IN750 (4.7v)

Form AEC-427
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